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TOPICAL REVIEW

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To cite this article: Jiaxiang Chen *et al* 2026 *Semicond. Sci. Technol.* **41** 073001

IOP Publishing   *Semicond. Sci. Technol.* **41** (2026) 073001   https://doi.org/10.1088/1361-6641/ae7ab3

Semiconductor Science and Technology

RECEIVED
31 December 2025

REVISED
21 March 2026

ACCEPTED FOR PUBLICATION
9 June 2026

PUBLISHED
6 July 2026

TOPICAL REVIEW

Recent advances in vertical β-Ga_2O_3 power devices: epitaxy, processing, and performance

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Keywords: gallium oxide, epitaxy, Schottky barrier diode, p–n junction, vertical transistor, reliability

Abstract

The growing demand for higher power density and operational frequency in power conversion systems is driving the development of devices that exceed the limits of conventional silicon. Beta-phase gallium oxide (β-Ga_2O_3) has emerged as a highly promising ultra-wide-bandgap semiconductor for next-generation high-voltage and high-efficiency power electronics. This promise stems from its exceptional material properties, including a large bandgap ($\sim$4.9 eV), a high theoretical critical electric field (8 MV cm^{-1}), and the availability of large-area, low-cost melt-grown substrates. These intrinsic characteristics facilitate vertical device architectures that can achieve unprecedented breakdown voltages while minimizing conduction losses. However, several key challenges currently limiting the application of vertical β-Ga_2O_3 devices must be addressed, including epitaxial quality, device degradation, low p-type doping efficiency, and inadequate thermal management. Overall, this review highlights the significant potential of vertical β-Ga_2O_3 power devices, which is being realized through rapid advancements in epitaxial growth, device fabrication, and defect control. Furthermore, achieving the full potential of β-Ga_2O_3 in high-power applications will require continued advances in p-type conductivity and thermal dissipation. The methodologies outlined may have broader applicability to other emerging semiconductor materials.

Contents

1. Introduction

The demand for power electronics has seen a consistent rise, driven by their implementation in sectors such as mobile communications, hybrid electric vehicles, and high-voltage direct current transmission. At the heart of these architectures lies the semiconductor switch, which functions as the essential operational component.

Silicon (Si) has historically maintained preeminence in the power device sector, underpinned by its established fabrication infrastructure, economic viability, and widespread availability. Nevertheless, as energy efficiency standards become more stringent and the demand for operation under high-power, elevated-temperature, and high-frequency regimes intensifies, the intrinsic physical constraints of Si are increasingly proving to be a prohibitive bottleneck. Wide-bandgap semiconductors, including gallium nitride (GaN), silicon carbide (SiC), and gallium oxide (Ga_2O_3), have emerged as promising alternatives to Si due to large bandgap and high critical electrical field. Notably, among all (ultra) wide-bandgap semiconductors, β-phase (β-Ga_2O_3) has gained significant recognition for developing the next generation of power electronics owing to its ultra-wide bandgap (4.9 eV) and large breakdown electric field of 8 MV cm^{-1} [1]. Its fundamental monoclinic crystal structure is depicted in figure 1. Besides, its estimated theoretical Baliga's Figure of Merit (BFOM) of 3.444 GW cm^{-2} is thousands of times higher than that of Si and superior even to SiC and GaN, making it an ideal platform for next-generation power electronics capable of handling high voltages and operating with reduced energy losses.

Beyond its superior electrical properties, β-Ga_2O_3 provides a crucial manufacturing advantage derived from its amenability to melt growth [2, 3]. As shown in table 1, for power electronics, this cost advantage over SiC arises from its inherently lower material cost and mechanical softness. Furthermore, the crucible cost is a major determinant of the total cost per β-Ga_2O_3 wafer [4].

High-performance β-Ga_2O_3 power devices require high-quality epitaxial layers on native substrates with precisely controlled doping, thickness, and low defect density to meet target breakdown voltages (BV), current ratings, and operating frequencies [2]. However, a pervasive challenge currently facing Ga_2O_3 is the effective suppression of defects, an issue that persists irrespective of the growth technique employed. Dislocations and grain boundaries are commonly present and degrade device performance and uniformity. Mitigating these issues requires optimization using high-quality, off-axis substrates and precise process management.

The development of vertical power devices has been accelerated by the availability of low-cost, large-size β-Ga_2O_3 substrates with controllable epitaxial thickness and doping profiles [5]. Compared with

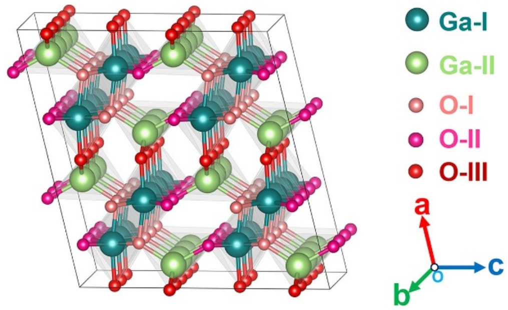

Figure 1. β-Ga_2O_3 crystal supercell structure based on its conventional unit cell.

Table 1. Comparison of key properties between β-Ga_2O_3 and other materials.

Features	Si	SiC	GaN	β-Ga_2O_3
HV device structure	Vertical	Vertical	Lateral	Vertical
Breakdown field strength	Low (0.3 MV cm^{-1})	Medium (2.5 MV cm^{-1})	Medium (3.3 MV cm^{-1})	High (8 MV cm^{-1})
Conductive loss	High	Medium	Medium	Low
Thermal conductivity	Medium (150 W m^{-1} K)	High (270 W m^{-1} K)	Medium (210 W m^{-1} K)	Low (10 $\sim$ 30 W m^{-1} K)
Cost	Low	High (10 $\times$Si)	Low (Si substrate)	Low (1/3 $\times$SiC)
Maturity	High	High	High	Low

lateral structures, vertical architectures offer superior area efficiency, a more uniform electric field distribution across the drift region and enhanced heat dissipation capabilities. These advantages make vertical devices a promising route toward high-voltage and high-current β-Ga_2O_3 power electronics. Vertical β-Ga_2O_3 power devices mainly include Schottky barrier diodes (SBDs), p–n heterojunction diodes (HJDs), and transistors. Despite breakthroughs in 10 kV-class devices [6–8], widespread commercial adoption of vertical Ga_2O_3 devices is constrained by persistent issues related to material quality, design optimization, and reliability.

The low efficiency of p-type doping and poor thermal conductivity of β-Ga_2O_3 constitute critical bottlenecks, especially for vertical devices operating at high power densities. The lack of efficient p-type doping in β-Ga_2O_3 makes it difficult to construct high-performance homogeneous p–n junctions [9]. This limits the realization of bipolar devices and results in insufficient surge withstand capability and electrical modulation flexibility, while restricting the further improvement of breakdown voltage and long-term reliability. Thus, the realization of Ga_2O_3 p–n junctions currently relies primarily on heterostructure configurations. For thermal management, the naturally low thermal conductivity of β-Ga_2O_3 (10–30 W m^{-1} K) severely limits the performance of β-Ga_2O_3 devices, making heat dissipation one of the major bottlenecks for future applications [10]. Within vertical devices, heat is generated throughout their volume rather than just at the surface. This configuration offers greater flexibility in developing thermal management solutions, such as heat sinks or cooling systems, which are essential for maintaining optimal operating temperatures and ensuring reliable performance.

This review presents a comprehensive overview of recent advancements in vertical β-Ga_2O_3 power electronics, encompassing epitaxial growth, device architectures, and emerging technical opportunities. The discussion begins with a critical examination of major epitaxial growth techniques, including halide vapor phase epitaxy (HVPE), metal–organic chemical vapor deposition (MOCVD), and molecular beam epitaxy (MBE). Subsequently, we analyze state-of-the-art vertical power devices—specifically SBDs, HJDs, and transistors—with a focus on current performance benchmarks and device reliability. Finally, the review addresses existing technical limitations and future perspectives. Ultimately, this work aims to provide a strategic roadmap to overcome current barriers, thereby accelerating the commercialization of high-performance vertical Ga_2O_3 devices for next-generation efficiency power systems.

2. Ga_2O_3 epilayer growth

Research on the epitaxy of β-Ga_2O_3 has advanced rapidly, with the benchmark for mobility versus carrier concentration shown in figure 2. High-quality Ga_2O_3 material plays a critical role in the fundamental of power electronics. β-Ga_2O_3 epitaxial thin film that can be grown by various techniques,

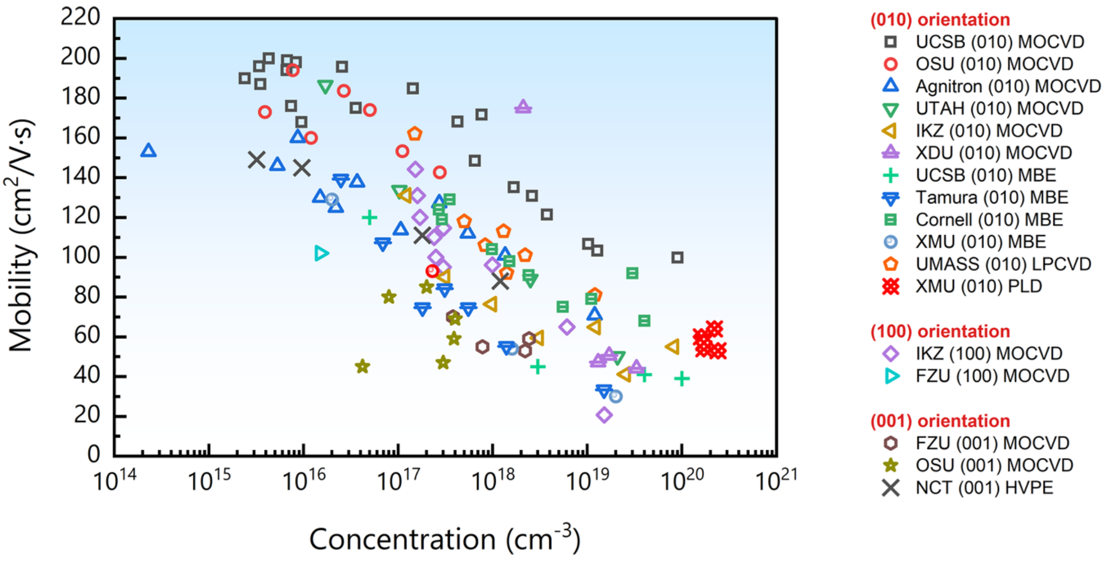

Figure 2. Benchmark of electron mobility and concentration of β-Ga_2O_3.

Table 2. β-Ga_2O_3 common growth methods.

Method	Orientation	Growth rate (μm h^{-1})	References
HVPE	010	25	[11]
HVPE	c-sapphire	250	[12]
HVPE	001	5	[13]
HVPE	011	16.4	[14]
MOCVD	001	10	[15]
MOCVD	010	3	[16]
MOCVD	010	16	[17]
MOCVD	100	1.5	[18]
MOCVD	−201	0.7	[19]
MOCVD	011	5.5	[20]
MBE	100	0.01	[21]
MBE	001	0.085	[21]
MBE	010	1	[22]

Table 3. Comparison of several typical Ga_2O_3 growth methods.

Growth	Growth rate	Crystal quality	Production efficiency	Scalability	Vertical device suitability	Challenge
HVPE	High	Good	High	Excellent	Excellent	• Low surface roughness • Low background concentration
MOCVD	Medium	Excellent	Medium	Excellent	Good	• Fast growth rate
MBE	Low	Best	Low	Poor	Poor	• Fast growth rate

including HVPE, MOCVD, low pressure chemical vapor deposition (LPCVD), MBE, pulsed laser deposition and atomic layer deposition (ALD). Among these approaches, HVPE and MOCVD are regarded as promising candidates for commercial Ga_2O_3 device fabrication, whereas MBE is mainly applied for the high-quality thin film growth. A detailed summary of these growth methods is listed in tables 2 and 3. HVPE achieves the highest growth rate (over 10 μm h^{-1}), making it highly suitable for thick film epitaxy. However, precise control over surface roughness and crystalline quality remains challenging. MOCVD typically provides growth rates in the range of 0.1–16 μm h^{-1}, achieving a favorable balance between film thickness and material quality. Nevertheless, simultaneously realizing high growth rates for thick films while maintaining excellent material quality presents an ongoing challenge. In contrast, MBE exhibits a relatively slow growth rate (below 1 μm h^{-1}), making it ideal for high-quality thin film growth and fundamental mechanism studies, despite its limited thickness scalability.

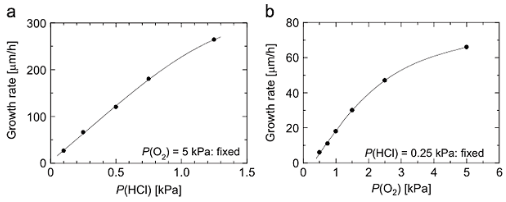

Figure 3. β-Ga_2O_3 growth rate as a function of HCl and O_2 partial pressure via HVPE. Reprinted from [12], Copyright (2015), with permission from Elsevier.

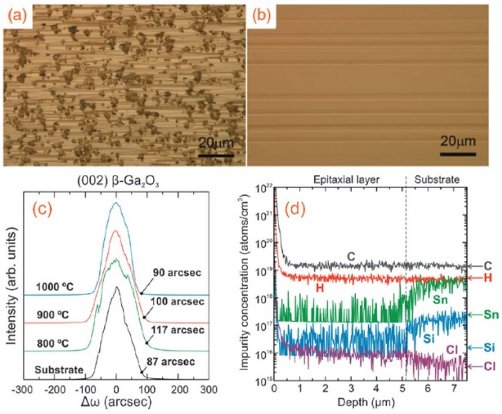

Figure 4. Characterization of HVPE-grown (001) β-Ga_2O_3 epilayer: Micrograph of the surface of β-Ga_2O_3 film grown (a) at 800 °C for 1 h and (b) at 1000 °C for 1 h; (c) XRD rocking curves of (002) diffraction plane at various temperatures; (d) SIMS depth profiles of an HVPE β-Ga_2O_3 film grown at 1000 °C. Reproduced from [13]. © IOP Publishing Ltd All rights reserved.

2.1. HVPE

HVPE, a critical technique for β-Ga_2O_3 epilayers, features ultra-high growth rates (typically larger than 10 μm h^{-1}) and high-purity films with low background carrier concentrations, serving as the mainstream method for thick drift layers in high-voltage vertical power devices.

The first report on the application of HVPE for β-Ga_2O_3 epitaxy emerged in 2014 [23], driven by the anticipation of achieving high growth rates and high-purity homoepitaxial β-Ga_2O_3 due to the success previously demonstrated in the growth of high-purity GaN and ZnO [24]. Detailed thermodynamic analyses established the foundational understanding for HVPE in β-Ga_2O_3 power device applications, specifically detailing the selection of precursors, carrier gases, and the optimal VI/III ratio. A typical HVPE system comprises a reactor chamber, precursor/carrier gas supply systems, a heating system, a substrate holder, and an exhaust treatment system. The reactor adopts segmented heating: the upstream zone (∼850 °C) facilitates GaCl formation via Cl_2/HCl reaction with high-purity Ga, while the growth zone (900 °C–1050 °C) enables β-Ga_2O_3 film deposition through GaCl–O_2 reaction, and $SiCl_4$ is typically used as the n-type dopant [23, 25].

HVPE holds a paramount advantage of a fast growth rate, normally in conditions of mass transport limitation, where the growth rate is proportional to the partial pressure of GaCl, with values ranging from several to hundreds of microns per hour. As shown in figure 3, Oshima *et al* achieved a growth rate exceeding 250 μm h^{-1} on a sapphire substrate using HVPE [12], and the growth rate increases linearly with the HCl and O_2 partial pressures.

As shown in figure 4, at a growth temperature of 1000 °C, a growth rate of 5 μm h^{-1} was achieved by Murakami *et al* while maintaining excellent crystal quality comparable to that of the substrate, as confirmed by x-ray diffraction (XRD) analysis. Furthermore, secondary ion mass spectrometry (SIMS) measurements revealed extremely low residual impurity concentrations and electrical measurements performed on the epilayer of SBDs inferred a background electron concentration of 10^{13} cm^{-3}, based on *C*–*V* measurements [13]. Konishi *et al* investigated the thermodynamics of HVPE-grown β-Ga_2O_3 films with different oxygen sources (O_2 and H_2O) through theoretical and experimental studies. Their experiments demonstrated that with optimized conditions, both oxygen gas and water can achieve growth rates of several μm h^{-1}. The growth rate using O_2 as the oxygen source are higher, exceeding 8 μm h^{-1}, while using H_2O yields smoother surfaces [26].

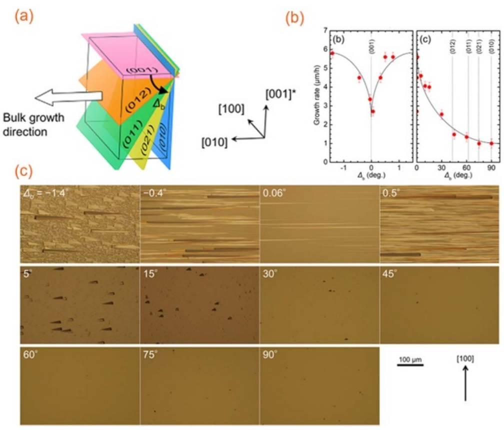

Figure 5. Effect of crystal planes on HVPE epitaxial β-Ga_2O_3: (a) schematic of different plane geometries of β-Ga_2O_3; (b) orientation dependence of the growth rate near the (001) plane and from the (001) to the (010) plane; (c) microscope photos of β-Ga_2O_3 films surface at different $\Delta\beta$. Reprinted from [29], with the permission of AIP Publishing.

The HVPE-grown β-Ga_2O_3 layer primarily utilizes Si^{4+} doping to achieve n-type characteristics. Experimental studies and actual growth data on doping control clearly demonstrate that the core advantage of high growth rates in HVPE does not significantly compromise the precision and uniformity of n-type doping. Goto *et al* employed $SiCl_4$ as a dopant precursor to perform *in-situ* n-type doping on HVPE-grown β-Ga_2O_3. The results demonstrated that by controlling the partial pressure of $SiCl_4$, electron concentration could be precisely regulated within the range of 10^{15}–10^{19} cm^{-3} at a characteristic growth rate of 5 μm h^{-1}. Electrical characterization revealed exceptional transport properties, and a mobility of 145 cm^2 $(V{\cdot}s)^{-1}$ was achieved at an electron concentration of 9.6×10^{15} cm^{-3} at room temperature, which further increased to 5000 cm^2 $(V{\cdot}s)^{-1}$ at 80 K [27]. The results confirm that HVPE holds advantages not only in growth rate and doping controllability but also in the superior electrical characteristics of the doped films. Based on these findings, Thieu *et al* prepared 2-inch (001) β-Ga_2O_3 epilayer, with a thickness of 10.9 μm and an electron concentration of 2.7×10^{16} cm^{-3} at a characteristic growth rate of 3–4 μm h^{-1}. XRD confirmed that the epitaxial layer's crystalline quality was comparable to the substrate, and electrical property measurements of the SBD device demonstrated the good uniformity of wafer [28].

The low symmetry and anisotropy of β-Ga_2O_3 result in distinct HVPE epitaxial behaviors on different substrate orientations. Goto *et al* compared the properties of β-Ga_2O_3 homoepitaxy on substrates with different off-angles ($\Delta\beta$), from the (001) ($\Delta\beta = 0°$) to the (010) ($\Delta\beta = 90°$) [29]. The results indicate that the film growth rate decreases significantly with increasing $\Delta\beta$, indicating that HVPE epitaxy on (001) plane becomes the current mainstream choice. Besides, the striped grooves observed on the (001) substrate also exhibit a close correlation between the depth and $\Delta\beta$, evolving into triangular pits as $\Delta\beta$ increases. A homoepitaxial layer free of pits was successfully grown when $\Delta\beta$ was around 60°, corresponding to the (011) plane, as shown in figure 5. Commercial HVPE β-Ga_2O_3 epilayers are typically grown on (001) substrates with an off-angle of approximately 0.1°, resulting in surface groove depths reaching up to 40% of the epilayer thickness [2].

As surface planarization via chemical mechanical polishing (CMP) is essential, the (011) orientation has garnered attention as a promising alternative to (001). Oshima *et al* investigated homoepitaxy on (011) substrates grown by HCl-based HVPE, and realized epilayers with higher growth rates than Cl_2-based HVPE and free of polycrystalline defects [14]. Figure 6 shows AFM and SEM images of the epilayer, revealing a smooth surface and uniform thickness. More importantly, the Cl impurity concentration within the (011) epilayer was measured to be approximately 1.7×10^{15} cm^{-3}, one order of magnitude lower than that in the (001) epilayer, a difference that is crucial for reducing the background electron concentration since Cl acts as a donor within β-Ga_2O_3. This study demonstrates the potential of the (011) orientation for low-cost, high-quality β-Ga_2O_3 epitaxial layers.

In addition to the mainstream (001) and the promising (011), studies of alternative orientations have also been attempted. Leach *et al* investigated HVPE homoepitaxy via HCl as a precursor on a (010) substrate with an off-angle of 2° [11]. By adjusting the O_2/GaCl ratio and partial pressure, a growth rate exceeding 25 μm h^{-1} was achieved with good film morphology. Ye *et al*also investigated HVPE-grown (010) β-Ga_2O_3 homoepitaxy and successfully suppressed the formation of surface hillock morphology

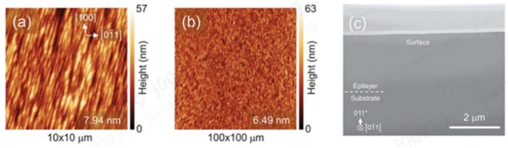

Figure 6. HVPE epitaxial (011) β-Ga_2O_3 epilayer surface: (a, b) AFM images of (011) epilayers at different scanning ranges; (c) STEM image of (011) epilayer/substrate interface. Reproduced from [14].

through process parameter optimization [30]. Besides, Butenko *et al* were the first to systematically compare HVPE homoepitaxial growth of β-Ga_2O_3 on substrates with (100), (–201), and (010) orientations [31]. Their results demonstrated that HVPE homoepitaxy of β-Ga_2O_3 is highly sensitive to substrate orientation: growth on the ($-$201) plane exhibits the highest growth rate ($>$10 μm h^{-1}). In contrast, the (100) plane shows the lowest growth rate ($\sim$0.5 μm h^{-1}) and the largest surface roughness. Growth on the (010) plane yields lower growth rates and crystal quality than those on ($-$201), but provides a comparatively smoother surface morphology, which can be further improved through multiple growth runs. These studies underscore the potential of (010) and ($-$201) plane in future HVPE epitaxy, which warrants further in-depth research.

However, the large equilibrium constant for β-Ga_2O_3 formation is considered as a key challenge in HVPE, which readily leads to the formation of β-Ga_2O_3 particles in the gas phase before reaching the substrate. These particles degrade film quality, hinder subsequent growth, and act as sources of defects, thereby restricting the growth rate of commercial Cl_2-based HVPE β-Ga_2O_3 wafers to 5 μm h^{-1}. To mitigate this issue, Ema *et al* optimized the process by developing tri-HVPE (THVPE), employing $GaCl_3$ as the gallium source for β-Ga_2O_3 homoepitaxy [32]. Through appropriate adjustment of the partial pressures of the first and second chlorides and oxygen source, they achieved a growth rate exceeding 6 μm h^{-1}, with the β-Ga_2O_3 film maintaining substrate-level quality. Notably, the THVPE-grown film surfaces showed no significant particle formation compared to HVPE, indicating that THVPE effectively suppresses gas-phase reactions, thereby improving the β-Ga_2O_3 film morphology and quality, as illustrated in figure 6. Subsequently, Nitta *et al* further improved the THVPE technique by directly employing a solid $GaCl_3$ precursor for β-Ga_2O_3 epitaxy [33]. The improved THVPE method demonstrated the capability for exceptionally high growth rates, surpassing 100 μm h^{-1} with specific conditions, while maintaining substrate-level crystalline quality in the epitaxial films.

With the widespread adoption of HVPE in the fabrication of β-Ga_2O_3 wafers and devices, the study of defects in HVPE-grown β-Ga_2O_3 epilayer has become increasingly important, as defects can significantly impact device performance. Stacking faults in HVPE-grown (001)-oriented β-Ga_2O_3 films are considered as killer defects, which may originate from stacking errors on (111) and (1–11) planes, manifesting as heart-shaped etch pits oriented toward the [34] direction [35]. Additionally, polycrystalline defects and linear-shaped defects have been observed, leading to an increase in device leakage current [36, 37]. As shown in figure 7, the stacking fault, line-shaped defects and polycrystalline defects are identified in the HVPE epilayer which primarily originate from the defect evolution at the substrate/epilayer interface and the incorporation of β-Ga_2O_3 powder particles generated during the HVPE growth process. Precisely controlling growth conditions, particularly by optimizing gas flow rates and appropriately reducing chamber pressure, can significantly reduce particles formed during the gas-phase pre-reaction, thereby minimizing epitaxial defects. The killer defect density on current commercial 4 inch HVPE wafers can be suppressed to less than 1 cm^{-2} [38], providing support for the development of high-performance devices.

In brief summary, HVPE has emerged as a pivotal growth technology for β-Ga_2O_3. Through scientific engineering optimization, it has matured into a technique capable of simultaneously achieving high growth rates and high crystal quality. Additionally, HVPE holds the ability to heterogeneously grow metastable phases of Ga_2O_3 besides the beta phase, such as the alpha and kappa phases (α- and κ-Ga_2O_3) [39, 40], which can be achieved on suitably matched substrates with high quality. The synergy between HVPE and β-Ga_2O_3 melt-grown substrates establishes a complementary pair, collectively building a foundation for low-cost, high-performance β-Ga_2O_3 semiconductor manufacturing. The previously challenging issue of Cl impurities and deep surface grooves in (001) epitaxy was effectively mitigated by changing to the (011) plane. It is plausible to anticipate that HVPE will become the key technology driving the advancement of high-voltage β-Ga_2O_3 devices.

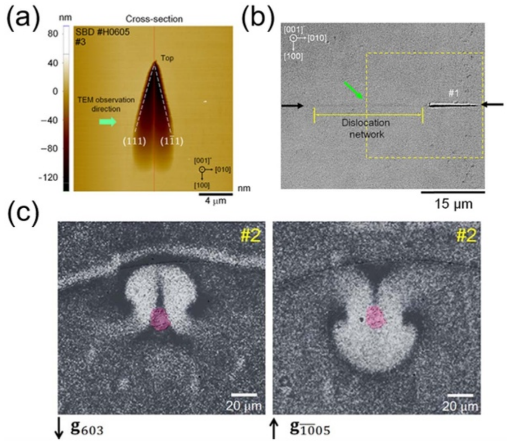

Figure 7. Characterization of defects in HVPE grown (001) β-Ga_2O_3 epilayers: (a) AFM image of etch pits formed at stacking faults after etching, appearing as a heart-shaped etch pit pointing in the (100) direction, composed of (111) and (1–11) stacking faults. Reprinted from [35], with the permission of AIP Publishing. (b) DICM image of line-shaped defect. Reproduced from [36]. © IOP Publishing Ltd All rights reserved. (c) Synchrotron x-ray topography images (black and white contrast) of SBD with diffraction vectors, overlapped with the DICM image of polycrystalline defect. Reprinted from [37], with the permission of AIP Publishing.

2.2. MOCVD

MOCVD represents another pivotal technique for Ga_2O_3 epitaxy, offering superior film uniformity, precise compositional control, and significant scalability. Despite the relatively low growth rates (typically 1–2 μm h^{-1}), MOCVD remains the dominant method for high-performance lateral β-Ga_2O_3 devices, where precise thickness and interface control outweigh the need for very thick layers. Its intrinsic precision and uniformity make it indispensable for high-power device fabrication. In the MOCVD reactor, gaseous precursors such as TMGa or TEGa and O_2, N_2O, or H_2O are transported by carrier gases (N_2 or Ar) to a heated substrate [41, 42]. With suitable temperature and pressure, the precursors undergo pyrolysis and chemical reactions on or near the surface to form β-Ga_2O_3, and the gallium precursor strongly affects growth rate and film quality. Experiments showed a linear relationship between Ga source flow and growth rate [41, 43], indicating minimal parasitic reactions.

Among the two commonly used Ga metal–organic sources, TMGa often introduces carbon through methyl decomposition and H incorporation, resulting in background electron concentrations around 10^{15} cm^{-3}—higher than HVPE-grown films [43–45]. Increasing the growth temperature and oxygen flow rate can effectively suppress the introduction of carbon [46]. In contrast, TEGa reduces the introduction of carbon due to different pyrolysis chemistry. Moreover, it enables *in-situ* etching capability at high temperatures, where the Ga formed during decomposition reacts with Ga_2O_3 to produce volatile Ga_2O [47]. This combined capability allows patterning and regrowth in one chamber, advantageous for complex device architectures. Furthermore, research into novel precursors, such as Dimethylgallium Isopropoxide (DMGIP), has shown promise for MOCVD growth of β-Ga_2O_3 films [48].

Owing to the excellent precision in flow control, MOCVD exhibits superior accuracy in realizing n-type doping, where Si, Ge and Sn represent the most commonly employed n-type dopants. Doping sources include TEOS and SiH_4 for Si^{4+} [49, 50], GeH_4 for Ge^{4+} [51], and TESn for Sn^{4+} [52]. Si doping is preferred non-alteration of conduction band minimum (CBM) dispersion in β-Ga_2O_3, thereby preserving high electron mobility [53]. It has also been discovered that the unintentional incorporation of nitrogen (N) when utilizing N_2O as an oxygen source can act as a compensating impurity, effectively reducing the background electron concentration and increasing resistivity, which may even enable p-type doping. Homoepitaxial β-Ga_2O_3 films obtained by N-doping in MOCVD achieve the lowest reported electron concentration of 10^{14} cm^{-3} and a mobility exceeding 150 cm^2 $(V{\cdot}s)^{-1}$, while maintaining low surface roughness, as shown in figure 8 [54]. Given that stable p-type β-Ga_2O_3 has not yet been demonstrated, N-doped β-Ga_2O_3 layers were widely used as current blocking layers (CBLs) in devices, which will be discussed later.

The development of crystal growth technology has enabled large β-Ga_2O_3 substrates in (100), (010), (001), (−201), and (011) orientations. Researches indicate that MOCVD-grown (010) β-Ga_2O_3 films can achieve superior crystal quality while maintaining excellent electrical transport properties. Via doping control, electron mobilities exceeding 150 cm^2 $(V{\cdot}s)^{-1}$ have been achieved at electron concentrations in the 10^{15}–10^{16} cm^{-3}, with reported peak values of 160 [55], 176 [44], 184 [56], 190 [43],

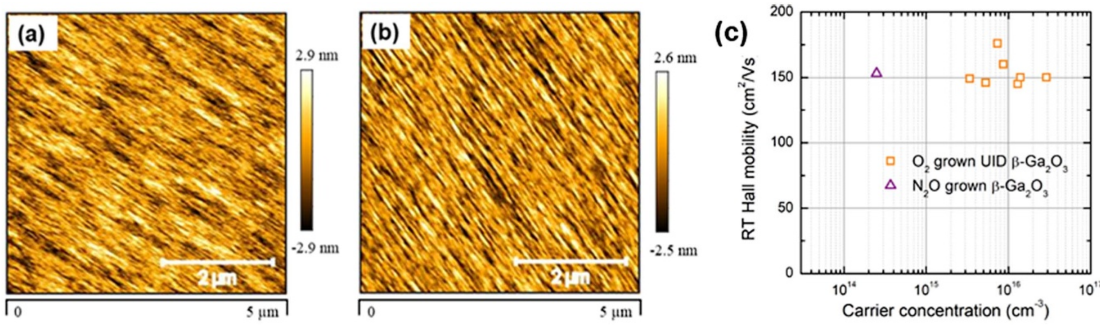

Figure 8. Characterization of N-doped (010) β-Ga_2O_3 films: AFM images of (010) β-Ga_2O_3 homoepitaxial films using oxygen (a) and N_2O (b) as gallium source. Room temperature Hall mobility for the N_2O grown film as compared to the latest pure oxygen grown unintentionally doped β-Ga_2O_3 is shown in (c). Reproduced from [54].

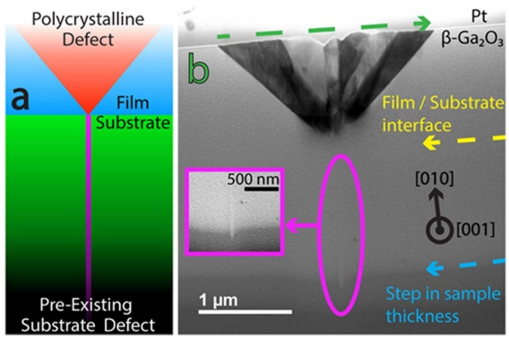

Figure 9. Sympetalous defect consisting of a nanotube in the substrate and polygonal pyramid in the epilayer film. (a) Cross section schematic and (b) TEM. Reprinted from [59], with the permission of AIP Publishing.

194 cm^2 $(V{\cdot}s)^{-1}$ [57]. Recently, Peterson *et al* achieved a maximum mobility of 200 cm^2 $(V{\cdot}s)^{-1}$ at a background electron concentration of 10^{15} cm^{-3}, close to the mobility limit at room temperature [58].

However, surface polycrystalline defects—multi-faceted pyramids induced by substrate nanotube defects that disturb step-flow growth are often developed in (010) epilayers [59]. Figure 9 presents a schematic diagram of the defect and the corresponding TEM image. Therefore, improving substrate quality plays a crucial role in achieving high-quality (010) epitaxial layers, which can also be mitigated by introducing substrates with appropriate off-angles.

In addition to (010), research on β-Ga_2O_3 epitaxy about (100) plane via MOCVD have also been widely conducted. For the (100) plane, low surface energy leads to 3D island growth and frequent twinning, which can be mitigated by adjusting process parameters or using substrates with large off-angles. For instance, by optimizing MOCVD parameters, Lu *et al* achieved (100)-oriented β-Ga_2O_3 film with a step flow growth mode on an on-axis substrate with root-mean-square (RMS) roughness of 0.238 nm [60]. Alternatively, employing substrates with off-angles provides additional adsorption sites for atoms via the increased step edges, thereby promoting two-dimensional growth and enhancing film quality. Studies confirm that miscut along (100)-[00 − 1] aids in reducing twins and improving crystal quality [61]. Anooz and Chou *et al* studied the effects of off-angle and growth parameters on the surface morphology evolution, and obtained a high-quality (100) epilayer with uniform step-flow morphology on a substrate with a 4° off-angle, even with a thickness of several μm through experimental optimization [27, 62], as shown in figure 10. Moreover, the maximum mobility with an electron concentration of 5.7×10^{15} cm^{-3} reached 160 cm^2 $(V{\cdot}s)^{-1}$ [63]. Han *et al* successfully grew thick Si-doped β-Ga_2O_3 films on (100) substrates with 4° off-angle, maintaining a step-flow morphology with a RMS roughness of only 3.19 nm even at a thickness of 8 μm and supporting SBD comparable to HVPE-based devices [18]. It is worth mentioned that the MOCVD-grown layer did not undergo CMP, thus saving a post-processing step [18]. Recently, Lu *et al* combined MOCVD growth with machine-learning–assisted optimization to realize high-quality homoepitaxial β-Ga_2O_3 films on on-axis (100) substrates [64]. The resulting films exhibit an XRD rocking-curve full width at half maximum (FWHM) of 57 arcsec for the (100) and a stable step-flow surface morphology with an ultra-low surface roughness of ∼0.12 nm. This

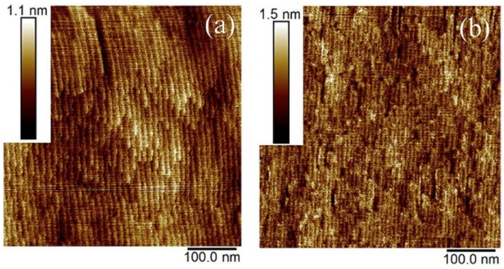

Figure 10. AFM images of homoepitaxial β-Ga_2O_3 films on (100) substrate with 4° off angles at different thicknesses: (a) 300 nm and (b) 3000 nm. Reproduced from [62]. CC BY 4.0.

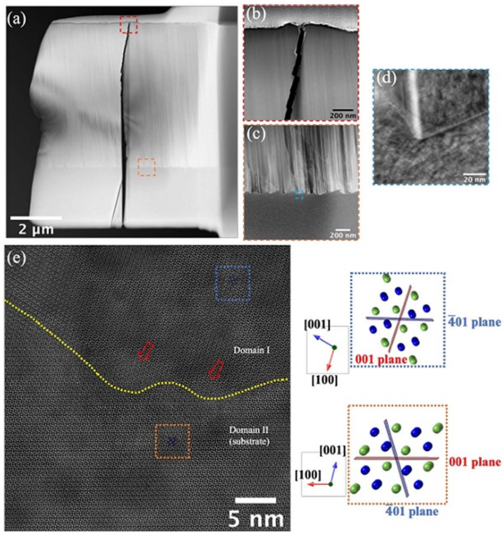

Figure 11. STEM images of (001) β-Ga_2O_3 film: (a) Cracking in the film; (b) zigzag at the interface; (c) High mag zigzag area; (d and e) rotation domains. Reprinted with permission from [45]. Copyright (2024) American Chemical Society.

work challenges the prevailing view that high-quality (100) homoepitaxy can only be achieved on substrates with large off-angles, thereby providing a viable pathway to reduce the cost of β-Ga_2O_3 materials and devices.

The (001) orientation of β-Ga_2O_3 is currently the mainstream orientation for thick films, with HVPE having demonstrated fast growth rates exceeding 10 μm h^{-1} on (001) plane. However, MOCVD on (001) β-Ga_2O_3 homoepitaxy presents difficulties. Meng *et al* investigated (001) β-Ga_2O_3 homoepitaxy using MOCVD. Their results showed that using TMGa as the precursor, the films were prone to cracking and exhibited (−401) rotation domains at high growth rates and thicknesses, as shown in figure 11 [45]. This investigation underscores the critical importance of rigorously optimizing growth parameters. By reducing growth rate, Zhao *et al* successfully grew a 5 μm thick (001) β-Ga_2O_3 film at a growth rate of 1.0 μm h^{-1} [65]. The resulting film surface showed a stable step flow morphology with an RMS roughness of only 0.98 nm and the absence of cracks or rotation domains. Waseem *et al* achieved a 13-μm-thick (001) β-Ga_2O_3 epitaxial film via MOCVD with XRD revealing a (001) diffraction plane FWHM of only 34 arcsec, indicating superior crystal quality [66]. These results demonstrate the potential of MOCVD to achieve high quality thick films.

In addition to the three crystal orientations mentioned above, Li *et al* investigated MOCVD homoepitaxy of β-Ga_2O_3 films on the (−201)-oriented substrate, achieving high-quality single-crystal films with substrate-level quality and uniform surfaces [19]. Recently, (011) β-Ga_2O_3 epitaxial layers were successfully deposited on (011) substrates via MOCVD, exhibiting a fast growth rate (5.5 μm h^{-1}), outstanding crystalline quality, and smooth surface morphology with thickness of 20 μm [20]. Consequently, further investigation is required to identify the optimal crystallographic orientation for MOCVD growth.

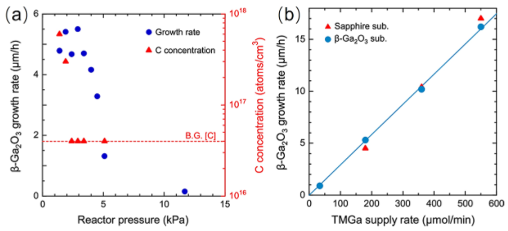

Figure 12. Effect of MOCVD parameters on growth rate: (a) the relationship between reactor pressure, growth rate, and carbon concentration; (b) linear dependence of the growth rate on the molar flow rate of TMGa. Reproduced from [17]. CC BY 4.0.

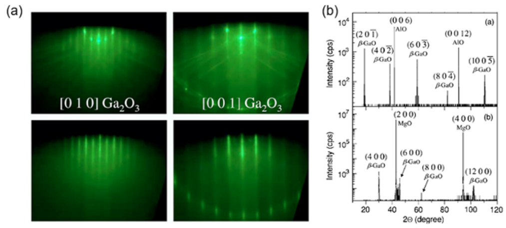

Figure 13. β-Ga_2O_3 growth on different substrates: (a) RHEED patterns of MBE-grown β-Ga_2O_3 films on (100) substrates; (b) XRD patterns of MBE-grown β-Ga_2O_3 heteroepitaxial films on c-plane sapphire and MgO substrates. Reprinted from [77], with the permission of AIP Publishing.

Like HVPE, MOCVD also enables the growth of metastable Ga_2O_3 phases such as α-, κ-, and ε-Ga_2O_3 by adjusting precursors and substrates [67–69]. Moreover, $(Al_xGa_{1-x})_2O_3$ alloys can be grown via MOCVD, allowing bandgap tuning and the creation of $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterojunctions with δ-doping. These supporting high-density two-dimensional electron gas (2DEG) channels, which is essential for HEMTs. Ranga *et al* reported on $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterojunctions grown by MOCVD, achieving an electron sheet charge density of 6.4×10^{12} cm^{-2} [70]. The parameters of MOCVD were optimized for this heterojunction epitaxy, resulting in further enhanced performance, yielding sheet charge densities ranging from 6.4×10^{12} cm^{-2}–1.06×10^{13} cm^{-2} and a maximum electron mobility exceeding 125 cm^2 (V·s)$^{-1}$ [71].

Although MOCVD is traditionally limited to relatively slow growth rates (<2 μm h^{-1}), recent progress has dramatically increased its speed through reactor innovations [72]. Agnitron's CCS MOCVD achieved >10 μm h^{-1} growth [73], and Taiyo Nippon Sanso's horizontal hot-wall system exceeded 16 μm h^{-1} with carbon impurity below SIMS detection limits [17], as shown in figure 12. Meng *et al* also achieved a growth rate of over 10 μm h^{-1} on the (001) substrate using MOCVD [15]. These technological advancements bring MOCVD throughput closer to that of HVPE, enabling deposition of thick films suitable for 5–10 kV devices.

2.3. MBE

MBE, operating in ultra-high vacuum with atomic-layer precision, is ideal for fundamental β-Ga_2O_3 research, heterostructure design, and high-performance device fabrication. Its primary advantage lies in precise interface control and accurate precursor flux adjustment, enabling high-quality β-Ga_2O_3 films, superlattices, and 2DEG channels. However, the inherently slow growth rate of conventional MBE limits its application in high-voltage vertical devices requiring thick layers, despite its excellence in fabricating lateral structures. For achieving high electron mobility, MBE serves as a promising technique for preparing heterostructure vertical devices, such as β-Ga_2O_3 HEMT-CAVETs [74]. Moreover, plasma-assisted MBE (PAMBE) nitridation and growth act as highly effective techniques for fabricating bipolar β-Ga_2O_3-based devices, typified by p-GaN/n-Ga_2O_3 vertical diodes [75].

In MBE systems for β-Ga_2O_3 growth, the gallium source is typically supplied by a standard effusion cell for heating high-purity elemental gallium metal, while the active oxygen source can be ozone or oxygen plasma [25, 76]. Villora *et al* first achieved MBE-grown β-Ga_2O_3 epilayer via PAMBE in 2006 [77]. High-quality homoepitaxy on (100) β-Ga_2O_3 substrates was grown, confirmed by distinct reflection high-energy electron diffraction streaks, as shown in figure 13(a). In contrast, heteroepitaxial films grown on c-plane sapphire and MgO substrates exhibited (−201) and (100) orientations, respectively, as shown in figure 13(b).

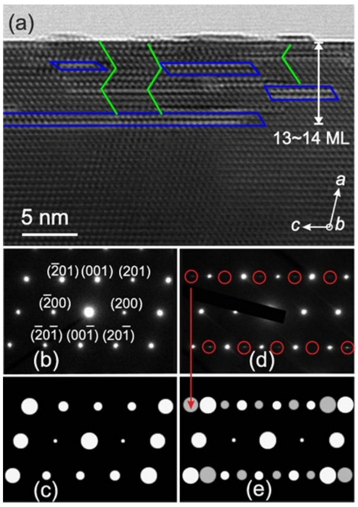

Figure 14. Characterization of twins in (100) β-Ga_2O_3 epilayers: TEM (a) depicts the homoepitaxial film. Twin domains and stacking faults are marked by green and blue lines, respectively. The electron diffraction patterns received at substrate (b) and the grown film (d) agree very well with the simulations in (c) and (e). Reproduced from [80].

Among all crystal orientations, the (010) plane is most widely used for MBE-grown β-Ga_2O_3 due to its symmetry, suppression of twins and stacking faults, and relatively high surface energy, which enhances adatom incorporation [21, 78]. Sasaki *et al* demonstrated a pronounced orientation dependence of the growth rate, reporting that homoepitaxy on the (100) plane was the slowest due to enhanced re-evaporation, whereas the (310) and (010) orientations exhibited the highest growth rates [21]. However, (010) epitaxial films may still contain surface defects, which are typically derived from imperfections in the underlying substrate [2].

Similar to MOCVD and HVPE, MBE epitaxy on (100) plane also leads to slow growth and promotes the formation of twin domains [79]. Cheng *et al* reported that MBE growth on the (100) plane resulted in a significant increase in twins and stacking faults within the epilayer compared to the substrate [80], as illustrated in figure 14. These defects stem from the coalescence of bi-oriented islands, a behavior like that observed in MOCVD growth, which can be alleviated by employing substrates with an intentional off-angle [81].

Epitaxy on other crystal orientations via MBE has also been reported. The (001)-oriented β-Ga_2O_3 has been grown with a growth rate of approximately 2.3 nm min^{-1}, second to that of the (010) orientation. The orientation remains stable at high temperatures, with crystal quality comparable to that of (010), showing no apparent defects and relatively smooth surfaces, making (001) a promising alternative orientation for high-quality device epitaxy [78]. In contrast, epitaxy on the (−201) plane requires lower growth temperatures or higher oxygen flux, resulting in a low rate and susceptibility to twins and surface roughness, often requiring optimization through substrates with miscut angles [78]. Conversely, MBE on the (110) face achieved a low RMS roughness of 0.08 nm and a growth rate comparable to (010). However, the film surface lacks a clear step-and-terrace structure [10]. Sasaki *et al* suggested that (010), (310), (301), (001), (−102), and (−401) are all suitable crystal orientations for MBE growth [2, 21]. Further research is required to determine the best orientation for specific device applications.

The growth rate of Ga_2O_3 through MBE is typically low, as the growth mechanism involves a two-step process when gallium is used as the source: adsorbed Ga and O react to form volatile Ga_2O, which then oxidizes to solid β-Ga_2O_3 [82]. The high vapor pressure of Ga_2O often limits the growth rate, and excessive desorption can even bring net etching [78, 83], analogous to the TEGa-induced etching in MOCVD. To overcome the slow growth inherent to MBE, two advanced approaches have been developed: Suboxide MBE (S-MBE) and Metal-Exchange Catalyzed Epitaxy (MEXCAT). The former directly supplies Ga_2O molecular beams to bypass the rate-limiting oxidation of Ga, significantly improving the growth rate [22], while the latter introduces catalytic metals (In, Sn) that accelerate β-Ga_2O_3 formation and suppress desorption [2, 84]. Through these innovations, MBE growth rates for β-Ga_2O_3 have been successfully increased to approach 1 μm h^{-1}, a rate comparable to that of MOCVD [22].

While MBE offers highly precise control via its intrinsic precision, precursor chemistry poses distinct challenges for different dopants. Sn is the most widely used dopant in MBE homoepitaxy, typically supplied from a SnO_2 source (K-cell), allowing for concentration control by adjusting the K-cell

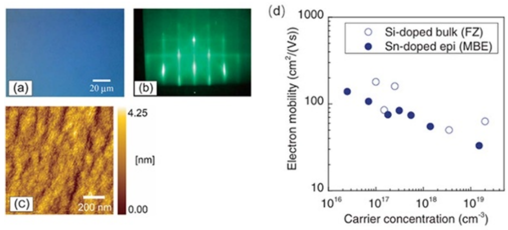

Figure 15. Characterization of MBE-grown Sn-doped (010) β-Ga_2O_3 films: (a) Nomarski microscope image, (b) RHEED pattern, (c) AFM of β-Ga_2O_3 film; (d) Electron mobility as a function of carrier concentration. Reproduced from [21].

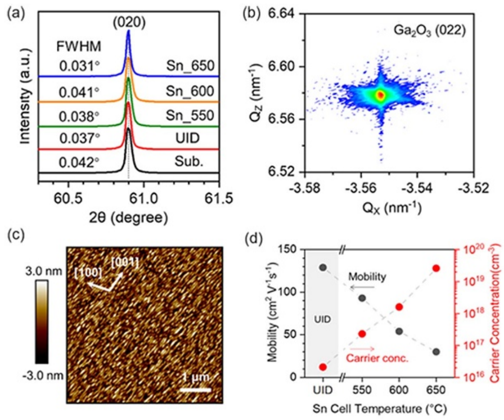

Figure 16. Characterization of MBE-grown Sn-doped (010) β-Ga_2O_3 films: (a) XRD patterns; (b) Reciprocal space mapping (RSM) around the β-Ga_2O_3 (022); (c) AFM; (d) Mobilities and carrier concentrations of the UID and Sn-doped films with different Sn cell temperatures. Reprinted from [85], Copyright (2024), with permission from Elsevier.

temperature. Sasaki *et al* achieved controllable Sn doping in (010) epitaxial β-Ga_2O_3 films with electron concentrations ranging from 10^{16} to 10^{19} cm^{-3} [21], with a maximum electron mobility exceeding 120 cm^2 Vs^{-1} and the surface roughness of the films of only 0.7 nm, as shown in figure 15. Similarly, high-quality (010) β-Ga_2O_3 homoepitaxial films grown by MBE exhibit a narrow XRD FWHM of 0.037° and a low RMS surface roughness of 1.07 nm. For UID films, the electron concentration was measured at 2.1×10^{16} cm^{-3}, with a maximum electron mobility of 129 cm^2 $(V\cdot s)^{-1}$ [85]. Figure 16 depicts the characterization results of MBE-grown β-Ga_2O_3 films.

Ge can also be used for n-type doping of β-Ga_2O_3 in MBE. Ahmadi *et al* achieved 10^{16}–10^{20} cm^{-3} doping with mobility over 120 cm^2 $(V\cdot s)^{-1}$ at low concentrations [86]. The Ge flux is strongly temperature-dependent, and achieving high doping concentrations typically requires growth temperatures lower than 600 °C, risking poorer crystal quality. Significant Ge segregation was observed within the top 2 nm of highly Ge-doped (010) films, which enhanced the surface conductivity. This study confirms that the over-doping technique can be leveraged as an effective method for achieving δ-doping to construct advanced HEMT devices, thereby converting this limitation into an advantage [87].

Si can be considered as a better donor compared to Ge and Sn, since it is predicted to be the only truly shallow donor among them. However, Si source oxidation poses critical issues to the control of Si doping in MBE [88]. This issue can be effectively addressed by using modified Si sources or their solid suboxides. To overcome this challenge, a modified Si source with a slanted aperture was adopted to mitigate oxidation, yielding controlled doping concentrations of 10^{17}–10^{20} cm^{-3} and an electron mobility of 125 cm^2 $(V\cdot s)^{-1}$ at 10^{17} cm^{-3} [89]. Moreover, by adopting SiO_2 as a solid source, S-MBE delivers a stable SiO beam, enabling wide-range Si doping (10^{16}–10^{19} cm^{-3}) and 124 cm^2 $(V\cdot s)^{-1}$ mobility [22].

Moreover, atomic-level precision of MBE makes it the preferred method for realizing $(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 heterostructures, which are crucial for the formation of 2DEG and the development of high-performance HEMTs. Zhang *et al* achieved $(Al_{0.18}Ga_{0.82})_2O_3$/$\beta$-$Ga_2O_3$ with a sheet density of 2×10^{12} cm^{-2}, mobility of 180 cm^2 $(V\cdot s)^{-1}$ at room temperature, and 2790 cm^2 $(V\cdot s)^{-1}$ at low temperature [90]. Kalarickal *et al* further increased carrier density to 4.7×10^{12} cm^{-2} by introducing a 1-nm-thick spacer layer, achieving a mobility over 150 cm^2 $(V\cdot s)^{-1}$ [91].

Table 4. Summary of the etching treatment and surface roughness of β-Ga_2O_3.

Orientation	Etchants	Etching method	Wet treatment	RMS (nm)	References
(010)	SF_6/BCl_3	RIE	NA	2.6	[102]
(−201)	SF6/Ar	ICP	NA	1.97	[104]
(001)	BCl_3/N_2	ICP-RIE	NA	0.65	[105]
(001)	BCl_3/Ar	ICP-RIE	H_3PO_4 at 130 °C	0.49	[106]
(001)	BCl_3/Cl_2	ICP-RIE	SPM (H_2SO_4/H_2O_2)	2.15	[98]
(001)	BCl_3/Cl_2	ICP-RIE	TMAH	0.21	[98]
(001)	BCl_3/Cl_2/Ar	ICP-RIE	BOE (HF/NH_4F)	0.12	[103]

The MBE technique for β-Ga_2O_3 growth yields ultra-low defect, high-purity epitaxial films with atomic-level thickness and doping profiles control. Additionally, the relatively low growth temperature facilitates advanced techniques such as selected-area or secondary epitaxy. However, the low growth rate (0.1–1 μm h^{-1}) limits thick drift layer fabrication for vertical power devices, while the high UHV equipment costs and large-area epitaxy challenges hinder large-scale commercialization. Nevertheless, MBE remains indispensable for advanced device architectures (e.g. lateral MOSFETs, HEMTs, quantum structures) that requiring superior hetero-interfacial quality, thereby ensuring its pivotal role in Ga_2O_3-based device.

3. SBD

3.1. Schottky contact and surface treatment

Depending on the work function difference and interface states between metal and semiconductor, metal–semiconductor contacts can form either Schottky contact or ohmic contacts. The rectifying behavior, which highly depends on the quality of Schottky contact, holds critical influence on device operation in RF and power applications. To tailor the Schottky barrier height and enhance contact Schottky stability, various metals have been investigated, such as Ni [92], Pt [93], Au [94], W [95], and TiN [96].

Appropriate surface treatment is considered as a promising approach to improve Schottky contact quality, such as etching [97], wet-solution [98], plasma [34, 99], annealing treatments [100] and supercritical fluid (SCF) treatment [101]. A summary of the surface treatment techniques of Ga_2O_3 is shown in table 4. Although various surface treatment techniques have been investigated, achieving atomic-level surface roughness and step-flow morphology remains a challenge, especially for HVPE-grown Ga_2O_3 [102]. Wet-solution processing is conducive to repairing the surface damage caused by dry etching and lowering the surface roughness. The synergistic effect of dry and wet surface treatments is critical to achieving high-performance device. ICP etching followed by buffered oxide etch (BOE) solution treatment yielded a β-Ga_2O_3 epilayer with an RMS roughness of 0.12 nm and a step-flow morphology [97, 103]. Owing to the reduction of oxygen vacancies, this treatment led to enhanced breakdown voltage of SBDs.

Besides surface etching, plasma treatment and annealing are also utilized as promising approaches for surface modification and the improvement of interface quality. As reported [34], N_2O plasma treatment was successfully applied to the fabrication of β-Ga_2O_3 SBDs. During the N_2O plasma process, nitrogen atoms were incorporated into the β-Ga_2O_3 surface and formed Ga–N bonds, resulting in a thin N-doped high-resistivity layer that could effectively passivate oxygen vacancies and surface states. Relative to the pristine sample, the reverse leakage current was decreased by one order of magnitude, and the on/off ratio was elevated by nearly an order of magnitude to 5×10^{11}. Meanwhile, the breakdown strength was significantly increased due to the formation of the semi-insulating N-doped β-Ga_2O_3 surface layer, which redistributed the electric field and suppressed premature breakdown. For plasma and annealing treatment, the enhanced SBD with O_2 plasma and annealing treatment demonstrates a PFOM of 1.2 GW cm^{-2}, confirming the crucial role of surface pre-treatment in improving Schottky contact quality of the devices [99].

SCF processing for β-Ga_2O_3 devices remains in the preliminary stage. Specifically, SCF treatment (N_2O, 130 °C, 1 h) efficiently suppresses the leakage current of SBDs via the synergistic effect of trap passivation, reduced carrier concentration and increased SBH [101].

Overall, appropriate surface treatment is crucial for improving device performance and uniformity by reducing defects and suppressing surface states.

Table 5. Summary of ohmic contact of β-Ga_2O_3.

Metal	Orientation	Electron concentration (cm^{-3})	RTA (°C)	ρ_c (Ω cm^2)	References
Ti/Au/Ni	(010)	3×10^{20}	470	1.62×10^{-7}	[107]
Ti/Au	(010)	$\sim 10^{19}$	450	4.6×10^{-6}	[108]
Ti/Au	(010)	2.6×10^{18}	470	5.0×10^{-3}	[109]
Ti/Au	(010)	$\sim 10^{19}$	470	3.93×10^{-5}	[110]
Ti/Au	(001)	10^{18}	400	5×10^{-4}	[111]
Ti/Mg/Ti	(001)	10^{18}	400	6.25×10^{-4}	[112]
Cr/Au	(100)	$>10^{18}$	350	1.36×10^{-4}	[113]
TiW	(100)	10^{19}	700	1.5×10^{-5}	[114]

3.2. Ohmic contact

For β-Ga_2O_3 power devices, besides the quality of Schottky contacts, the high resistance at the ohmic contacts also persists as a key obstacle for fabrication of high-performance devices. Various methods, including ion implantation [108], regrowth [107], interfacial layer [115], and spin-on-glass [116] have been employed to achieve the low and stable contact resistance in β-Ga_2O_3 devices.

A summary of the ohmic contact on β-Ga_2O_3 is shown in table 5. Many studies have focused on a Ti contact layer with low work function, followed by an Au overlayer as the ohmic contact metal deposited by electron-beam evaporation [107, 108]. Rapid temperature annealing (RTA) is employed to form an effective ohmic contact by the diffusion and oxidization of Ti at the M-S interface which establishes an alloy compound layer at the interface of metal and Ga_2O_3. The interdiffusion of metal and the resulting thin Ti–TiO_x layer hold huge benefits for band alignment and carrier transport, leading to the reduction of the ohmic contact resistance. The ohmic contact shows orientation-dependence of Ga_2O_3. The Ti–TiO_x layer thickness of (100) substrate is much thinner than (010) substrate, due to surface energy differences, anisotropic reactivity, and anisotropic diffusion [117]. In comparison with (010) Ga_2O_3 substrate, the ohmic contact could be more easily formed on ($\bar{2}$ 01) and (001) Ga_2O_3 planes, possibly due to high surface energy and dangling bond density [111].

In the previous reports, Ti/Au and Ti/Au/Ni stacks exhibited a contact resistance as low as 4.6×10^{-6} and 1.62×10^{-7} Ω cm^{-2}, respectively, when deposited on the highly-doped Ga_2O_3 film [107, 108]. However, degradation of Ti/Au contact was observed when the annealing temperature exceeds 500 °C. Meanwhile, gold-based process holds the disadvantage of prohibitively expensive price and incompatibility with silicon-based processes for large-scale mass production. Therefore, Au-free electrodes for Ga_2O_3 with low ohmic contact resistance becomes a promising method for fabrication [112, 114]. A low ohmic contact resistance of 1.5×10^{-5} Ω cm^2 has been demonstrated by the utilization of the refractory metal alloy TiW on highly doped β-Ga_2O_3 with annealing at 700 °C in nitrogen [114]. Meanwhile, existing vacancies, defect states or Ga impurities in this interlayer may also lead to a reduction in ohmic contact resistance.

3.3. Edge-termination techniques for SBDs

β-Ga_2O_3 SBDs exhibit outstanding characteristics of high breakdown voltage, low conduction loss, and superior power efficiency. Consequently, β-Ga_2O_3 SBDs are considered as strong candidates for power rectifiers, elements in converters, and switching devices in high-voltage, high-power electronic and energy conversion systems. To date, most studies on β-Ga_2O_3 SBDs have been based on devices fabricated from HVPE-grown materials, while progress on MOCVD-grown counterparts lags behind [18].

In terms of SBD device performance, the localized electric-field crowding at the anode edge induces premature breakdown, preventing the device from reaching the ideal field strength of β-Ga_2O_3. Therefore, edge-termination technique, such as mesa, field-plate (FP), trench, and junction termination extension (JTE), have been developed to improve the BV of β-Ga_2O_3 SBD.

3.3.1. Mesa termination and field plate

The mesa termination technique is highly attractive for its simple, self-aligned fabrication process. Nevertheless, conventional mesa structures inherently suffer from electric field crowding at the anode edge, which can limit breakdown performance. This issue can be mitigated through structural modifications, such as the integration of field plates, or by adjusting material properties, for instance, increasing the Schottky barrier height.

Most mesa termination studies are based on β-Ga_2O_3 SBDs grown on (001)-oriented substrates by HVPE. Wan *et al* [118] reported a β-Ga_2O_3 SBD with a FP-assisted deep mesa termination (FPDM) structure. The FPDM-SBD showed an impressive BV of 2510 V and a specific on-resistance ($R_{on,sp}$)

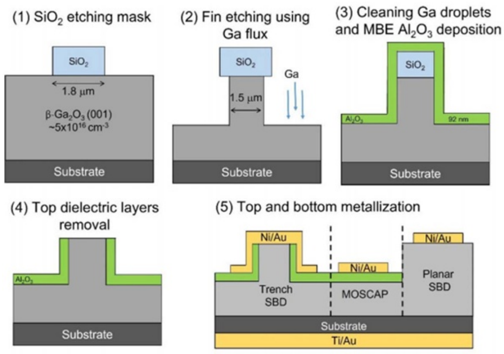

Figure 17. Process flow for the Ga-flux etched trench SBDs with low damage. Reprinted from [122], with the permission of AIP Publishing.

of 3.78 mΩ·cm^2, corresponding to a PFOM of 1.65 GW cm^{-2}, demonstrating the excellent trade-off between breakdown capability and conduction performance caused by the FPDM design. Han *et al* [119] reported a β-Ga_2O_3 SBD with another technique donated as suspended field plate-assisted shallow mesa termination (SFPM). A 200 nm-thick Ni layer was subsequently deposited both as the anode electrode and hard mask for self-aligned mesa etching. Cl_2 was introduced to promote isotropic etching during the mesa etching step, allowing the simultaneous formation of the suspended field plate along with the mesa termination. The resulting SFPM-SBD exhibited excellent electrical performance with a low $R_{on,sp}$ of 5.77 mΩ·cm^2 and a high BV of 3.5 kV, contributing to a high PFOM exceeding 2.12 GW cm^{-2}, demonstrating the great potential of the SFPM termination structure for high-voltage β-Ga_2O_3 power devices.

Research on SBDs with MOCVD-grown epilayers is also progressing rapidly. Vertical SBDs featuring mesa termination with a partially suspended field plate were fabricated on an 8 μm MOCVD-grown (100) β-Ga_2O_3 epitaxial film. Owing to the high-quality epilayer and effective electric field management at the device edge, the SBD exhibits a high BV of 3.45 kV and a low $R_{on,sp}$ of 3.88 mΩ·cm^2 [18]. FP SBDs were fabricated on a 6.5 × 10^{15} cm^{-3} intentionally doped 10 μm (010) MOCVD-grown thick film. The diodes were found to have high-quality anode metal/semiconductor interfaces with an ideality factor of 1.04, and a maximum breakdown voltage of 1.50 kV [120].

3.3.2. Trench termination SBD

In contrast to non-termination SBDs, trench SBDs demonstrate remarkable improvements in current density, BV, and $R_{on,sp}$ owing predominantly to their unique vertical trench configuration. Li *et al* [121] reported a β-Ga_2O_3 vertical trench SBD, which consists of fins with widths of 1–4 μm and a depth of 1.55 μm. The fins were formed by BCl_3/Ar-based dry etching and the hard mask of Ti/Pt, followed by wet etching to achieve a smooth and rounded trench corner that mitigates field crowding. The fabricated trench SBD obtains a high BV of 2.44 kV and a specific $R_{on,sp}$ of 11.3 mΩ·cm^2, demonstrating excellent rectifying characteristics. The reverse leakage current density remained below 1 μA cm^{-2} up to breakdown, due to the reduced surface field effect provided by the trench geometry.

In fabrication, sidewall defects and severe roughness are inevitably induced in the trench etching process. To reduce the etching damage, a β-Ga_2O_3 trench SBD via a low-damage Ga-atomic beam etching technique was demonstrated [114], as illustrated in figure 17. The trenches were etched via a two-step Ga-atomic beam process in an MBE chamber. The Ga-atomic beam etching, a purely chemical etching mechanism based on the reaction between Ga and β-Ga_2O_3 to form volatile Ga_2O, enabled smooth sidewalls of fins and sharply defined trenches (∼1.2 μm deep) due to the absence of plasma-induced damage. After Ga-atomic beam etching, residual Ga droplets left on the SiO_2 surface were removed by HCl dipping (5 min, 37%). Subsequently, a 92 nm-thick Al_2O_3 dielectric layer was grown by PAMBE. The fabricated trench SBDs exhibited a $R_{on,sp}$ of 1.20 mΩ·cm^2 and a BV of 1.45 kV, deriving a high PFOM exceeded 2.0 GW cm^{-2}. With reverse bias, the trench SBD achieved an extremely low reverse leakage current (∼10^{-4} A cm^{-2}).

3.3.3. JTE

JTE, a highly efficient technique widely used in Si and SiC devices, can be implemented in β-Ga_2O_3 through heterojunction engineering with p-type semiconductors.

Table 6. Comparison of parameters for various SBD terminal structures.

Device structure	Anode radius (μm)	BV (kV)	$R_{on,sp}$ (mΩ·cm^2)	PFOM (GW cm^{-2})	Fabrication complexity	References
w/o	100	2.1	∼6	0.74	Low	[100]
w/o	40	1.72	2.25	1.32	Low	[127]
FP	75	2.3	250	0.02	Low	[128]
FP	25	2.1	6.9	0.63	Low	[129]
FP	30	1.93	3.1	1.2	Low	[99]
Mesa	50	2.74	7.33	1.02	Low	[130]
JTE	50	2.11	2.9	1.54	Medium	[123]
JTE	70	3	6.15	1.46	Medium	[131]
Trench	NA	2.1	11.3	0.39	High	[121]
Trench	NA	1.45	NA	2	High	[122]
Trench + FP	NA	2.89	10.5	0.8	High	[132]
Mesa + FP	90	3.5	5.77	2.12	High	[119]
Mesa + FP	90	6	3.4	10.6	High	[133]

Single-layer JTE structure can effectively suppress the peak electric field at the edge. Hao *et al* [123] reported a β-Ga_2O_3 SBD with a JTE technique by p-type NiO. A 220 nm-thick p-type NiO-JTE was deposited on the sample surface via magnetron sputtering followed by a liftoff process. During sputtering, hole concentration in the NiO layer was carefully adjusted by the O_2/(Ar + O_2) gas ratio, thereby optimizing the termination effectiveness. The fabricated SBDs exhibited a low $R_{on,sp}$ of 2.9 mΩ·cm^2 and a BV of 2.11 kV, leading to PFOM of 1.54 GW cm^{-2}. The optimized oxygen partial pressure effectively enhanced the NiO acceptor density, improving the depletion control at the anode edge, and thereby suppressing premature breakdown.

Compared to single-JTE, SBDs with a graded JTE structure by sputtering p-type NiO can effectively migrate the peak electric field from the outer edge to inner edge [124]. The multiple p-type NiO layers hold various lengths to enable a graded decrease in effective charge density away from the main junction. A bilayer resist (AZ701/PMGI) process was employed for precise NiO liftoff, enabling controllable bevel angles to alleviate surface electric-field crowding. The graded NiO-JTE SBD exhibited a $R_{on,sp}$ of 5.9 mΩ·cm^2 and a BV of 2.5 kV, corresponding to a PFOM exceeded 1 GW cm^{-2}, confirming the effective suppression of edge field crowding and enhancement of high-voltage capability by graded NiO termination.

During JTE device operation, the numerous interface traps will be positively or negatively charged, leading to high leakage current [125]. Thus, polarization charges from high-k dielectrics can effectively counteract the electric field generated by interface charges, leading to a more uniform electric field distribution. Thus, high-k dielectric like $BaTiO_3$ assisted JTE (BTO-JTE) technique for vertical β-Ga_2O_3 SBDs is another method to reduce the sensitivity of BV to interface charges [126]. In comparison with single-zone JTE, the BTO-JTE creates a more uniform electric field distribution with significantly reduced peak electric field at the edges of the Schottky junction or JTE.

As shown in table 6, typical representative termination structures for β-Ga_2O_3 SBDs including Mesa, FP, heterojunction, and trench terminations, exhibit distinct trade-offs between fabrication complexity and device performance. Both Mesa and FP terminations feature structural simplicity, which are favorable for fabrication. However, Mesa termination necessitates deep etching to effectively suppress the peak electric field at the junction edge, inevitably introducing etch damage that degrades device reliability. FP termination achieves efficient electric field suppression, yet its high-voltage application is strictly limited by the demand for dielectric materials with high-k and superior breakdown field strength, such as $BaTiO_3$.

Heterojunction termination enables damage-free electric field homogenization and excellent breakdown performance, but it is restricted by complex epitaxial growth and high interface defect density. Trench termination delivers the strongest *E*-field modulation, while suffering from severe sidewall etching damage and low fabrication yield. Owing to the inherent performance bottlenecks of single-type terminations, composite termination structures are proposed to synergistically integrate the merits of different architectures, thereby alleviating electric field crowding, and balancing BV and on-resistance for high-performance β-Ga_2O_3 power devices.

3.4. Reliability of β-Ga_2O_3 SBDs

The stability of β-Ga_2O_3 SBDs in high-voltage and harsh-environment applications is undermined by accelerated defect-driven degradation under electrical stress, high temperature, and irradiation. There are many deep-level defects in β-Ga_2O_3 determining the mechanisms of current flow in high electric fields through changing the charge occupation of defects and their possible migration [134].

Fortunately, not all defects lead to detrimental device degradation, like excessive leakage and premature breakdown. Therefore, it is crucial to locate and analyze the properties of killer defects [135], and establish the correlation between these defects and the electrical characteristics of devices. Deep-level transient spectroscopy (DLTS), deep-level optical spectroscopy (DLOS), photoluminescence spectroscopy (PL), x-ray photoelectron spectroscopy and low-frequency noise (LFN) are regarded as powerful nondestructive methods to characterize the trap properties [92, 136, 137]. It is crucial to bridge the fundamental gap between defects and device reliability with various types of stress.

3.4.1. Thermal and electrical effect

Due to the interface states at M/S interface and bulk traps in β-Ga_2O_3 bulk material, the reliability of SBDs still faces challenge, especially for thermal and electrical conditions [136, 138].

The thermal effects occurring during electrical breakdown will induce thermo-mechanical failure in Ga_2O_3 devices. In literature, fin diodes fabricated on (001) β-Ga_2O_3 substrates exhibited cracking along the [010] direction after destructive breakdown [120, 139]. This cracking was suggested to be due to thermo-mechanical failure of the (100) cleavage planes due to heat generation during breakdown.

Regarding high-temperature performance, the comparative experiments proved that SBDs with W/Au electrodes exhibited nearly identical *I–V* characteristics at both room temperature and 500 °C, whereas samples with Ni/Au electrodes suffered permanent degradation after high-temperature exposure [140]. Furthermore, the excellent thermal stability of Schottky contacts was studied even when operated at 500 °C [141], indicating that the β-Ga_2O_3 SBDs can function reliably in high-temperature environments with appropriate metal contacts [142]. β-Ga_2O_3 SBDs with JTE also demonstrate excellent high-temperature endurance and recovery capability in temperature range from 298 K to 548 K [143]. Notably, after being subjected to high-temperature stress at 473 K for 2 h, the BV of the SBD remained at 2.97 kV, yielding a PFOM of 0.98 GW cm^{-2}. Dynamic electrical performance of SBDs at cryogenic temperature have also been studied [92, 136]. Leakage current at 100 K is one order of magnitude lower than that at 300 K, demonstrating outstanding blocking performance at low temperatures. An electron trap (E_C-0.82 eV) was extracted from DLTS in a β-Ga_2O_3 epilayer, which is related to the device instability and Lorentzian hump in low frequency noise spectra.

Forward [144] and reverse bias [145] stress-induced degradation mechanism have also been investigated, and the trap evolution has also been proved to play a critical role in SBD performance degradation [92, 138]. Prolonged forward stress induces increased leakage current and decreased threshold voltage (V_{th}), which is attributed to an intrinsic trap—likely a gallium (Ga) vacancy-related trap [144]. Feng *et al* demonstrated large-area (3 × 3 mm^2) β-Ga_2O_3 SBDs with a BV of 1.5 kV, a $R_{on,sp}$ of 9.2 mΩ·cm^2, and a surge current capability of 58 A by employing dual field plates and nitrogen ion implantation [146]. After a −1 kV stress for 1000 s, the devices exhibited only a minimal 0.1 V V_{on} shift and a low $R_{on,sp}$ increase by just 1.4%.

3.4.2. Radiation effect

For space harsh environment application, significant global research attention is focused on the impact of various radiation sources, including heavy ions, protons, neutrons, and gamma rays, on β-Ga_2O_3 SBDs [147–149].

The carrier removal rates of Si, SiC, GaN and β-Ga_2O_3 are summarized in figure 18, with the data sourced from the literature [150–153]. Benefiting from its larger bandgap, β-Ga_2O_3 can withstand higher-energy irradiation than GaN and SiC [150, 153]. With comparable carrier removal rates, β-Ga_2O_3 demonstrates higher radiation hardness than GaN. For Ga_2O_3 material, the carrier removal rate is highest for alpha particles and decreases in the order of protons, neutrons, electrons, and gamma rays, which aligns well with the relative NIEL values of each radiation species.

High neutron fluence led to a reduction in forward current density by two orders of magnitude and an extremely high on-resistance property due to the radiation-generated considerable series resistance in the SBD [154]. The dynamic degradation was significantly suppressed at 100 K before and after proton irradiation [147]. With the condition of reverse bias, the irradiated SBD exhibits more serious dynamic degradation than the pristine one at 300 K, resulting from the traps induced by proton irradiation.

For power devices, the single-event burnout (SEB) voltage is also a primary reliability metric. SEB effects were observed in SBDs with heavy ion (Bi, Ta, and Kr ions) irradiation [155]. With increasing reverse bias over 600 V, the local temperature inside the device rises sharply to the melting point of the β-Ga_2O_3 material, leading to thermal burnout of the devices after neuron irradiation [156]. Concurrently, Li *et al* identified the reverse bias applied during irradiation as a key factor which causes

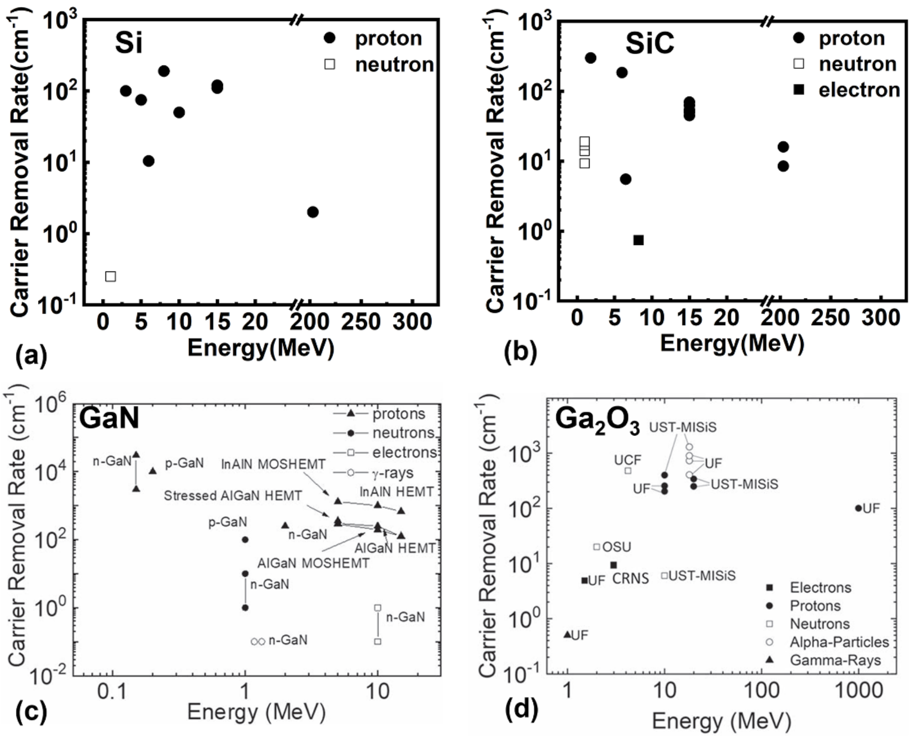

Figure 18. Summary of carrier removal rates for (a) Si, (b) SiC, (c) GaN and (d) β-Ga_2O_3. Reproduced from [153].

the failure of β-Ga_2O_3 SBDs. Their experiments revealed that applying a reverse bias of 400 V or higher during irradiation with 300 MeV high-energy protons could induce SEB [157]. The failure mechanism was attributed to the high local lattice temperature within the device reaching the melting point of β-Ga_2O_3, caused by energy deposition from secondary particles generated under high reverse voltage stress.

The recovery of the proton irradiation devices by post-annealing treatment was also investigated including partial recovery of carrier concentration and reduction of irradiation-induced defect [158]. Future research should focus on defect identification and annealing strategies to enhance radiation tolerance.

Moreover, ion implantation-based edge termination techniques can also cause lattice damage and induce traps in Ga_2O_3, while proper design will enhance the BV and reliability of SBDs. SBDs with F-implantation compound termination exhibit higher BV in forward electrical characteristics [159]. By optimizing the ion implantation and termination techniques, the uniformity of device are demonstrated to be enhanced [160].

3.4.3. Killer defect effect

Polycrystalline defects, stacking faults, probe-induced surface defects, line-shaped defects, and comet-shaped defects are typical killer defects in HVPE-grown (001) β-Ga_2O_3 SBDs, acting as leakage paths and causing premature breakdown [35, 161]. The investigation on homoepitaxy of β-Ga_2O_3 on alternative orientations such as (011) showed reduced killer dislocation formation because dislocations lied parallel to the (011) plane [162]. Hillock defects in MOCVD-grown (010) Ga_2O_3 SBDs also behave as killer defects that impair breakdown performance and need to be suppressed for high-voltage device application [120].

As device yield is directly governed by defect density, the suppression of killer defects becomes especially critical for large-area devices. In figure 19, for ampere-class SBDs, after etching away the surface dead layer containing traps, the breakdown characteristics were significantly improved, and the leakage mechanism of the SBD evolved from variable range hopping at medium reverse voltages to space-charge limited current (SCLC) at high reverse voltages [163].

Annealing and plasma processing also effectively mitigate the killer defect density. The BV of SBD is improved by over three times after 1000 °C oxygen annealing due to the inhibition of line-shaped killer defects. Nevertheless, this treatment reduces the carrier concentration and thus increases the $R_{on,sp}$.

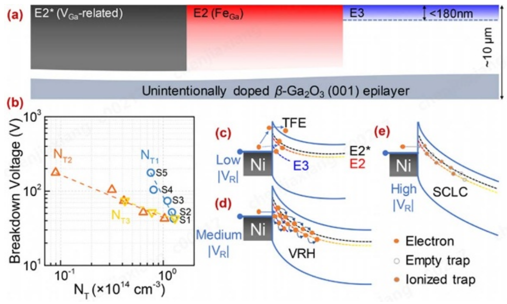

Figure 19. Schematics of the band diagram with the associated leakage mechanisms in β-Ga_2O_3 SBD dominated by traps. Reprinted from [163], with the permission of AIP Publishing.

Differently, Ar plasma treatment eliminates surface killer defects, achieving excellent performance uniformity in SBDs with varied areas [164], while also lowering the turn-on voltage and $R_{on,sp}$.

4. Vertical p–n HJDs

Compared with SBDs, p–n HJDs present significant advantages in lower reverse leakage current and higher reverse breakdown voltage, making HJDs superior for applications demanding high voltage and high reliability [165, 166]. Owing to the inherent limitation in p-type doping for β-Ga_2O_3 material [167], NiO_x [7, 8, 168–177], Cu_2O [178–181], SnO [182–184], Cr_2O_3 [185, 186], $CuCrO_2$ [187], diamond [188–190], hBN [191], GaN [75, 192–194], GaAs [195, 196], Si [197, 198] have been explored as promising candidates for fabricating β-Ga_2O_3 HJDs. In particular, significant advancements have been achieved in the development of NiO/β-Ga_2O_3 power rectifiers, surpassing the performance limitations observed in GaN and SiC structures, particularly in one-dimensional configurations [199].

4.1. β-Ga_2O_3 HJDs with p-type NiO

Oxide materials are considered as the preferred p-type semiconductor for forming p–n junctions with n-type β-Ga_2O_3 due to the absence of the interfacial oxidation reaction and the more convenient device fabrication processes [168]. Among all oxide materials, NiO, as a native p-type semiconductor, features a wide bandgap of 3.7 eV, excellent preparation compatibility and stability, controllable p-type doping, and a high mobility. More importantly, a Type-II band alignment can be formed at p-NiO/n-β-Ga_2O_3 interface, with ΔE_C exceeding 2 eV thus leading to excellent electron blocking, which showcase promising prospects for implementation in NiO/β-Ga_2O_3 heterojunction devices

Kokubun *et al* [168] pioneered the fabrication of *p*-NiO/β-Ga_2O_3 all-oxide p–n HJD. A Li-doped NiO epitaxial layer was grown on β-Ga_2O_3 substrates via the sol–gel method. The ideality factor was extracted to be approximately 2.0, indicating that the recombination current dominated the current flow process of HJDs. For wafer-level vertical β-Ga_2O_3 heterojunction rectifiers, NiO/Ga_2O_3 diodes fabricated on 4 inch diameter bulk Ga_2O_3 substrates with 10-μm-thick drift layers exhibit a median BV of $\sim$6 kV in the target region, while the regions with thinner drift layers and higher doping levels show a median BV of $\sim$3 kV [3]. Optimization of both thickness and doping uniformity is still needed.

A thicker epitaxial layer and a double-layer p-type material can further enhance the BV of Ga_2O_3 heterojunction p–n diodes. In figure 20, the BV can reach up to 13.5 kV in 100 μm-diameter NiO/Ga_2O_3 HJD, exceeding the 1D breakdown limit of both SiC and GaN with comparable drift layer thickness [7]. These diodes were fabricated by the lightly doped (8.8×10^{15} cm^{-3}) and thick (17–18 μm) Ga_2O_3 drift layers grown by HVPE, combined with low damage deposition of NiO and fabrication of dual layer field plates. A bilayer extension of the NiO layer beyond the metal contact provides a guard ring for additional edge termination. Furthermore, the simple device structure obviates the need for mesa etching or ion implantation steps, thereby minimizing ion-induced damage, optimizing the bevel angle at the diode edge to mitigate electric field crowding.

The hetero-interface quality determines not only the device performance but also the long-term reliability. Similar to SBDs grown on HVPE, the residual contaminants from slurry and/or the CMP-related defects can potentially degrade β-Ga_2O_3 surface. Thus, a proper post-CMP surface control process is also highly desirable before fabricating β-Ga_2O_3 HJD, such as surface etching [200], plasma treatment [170, 171].

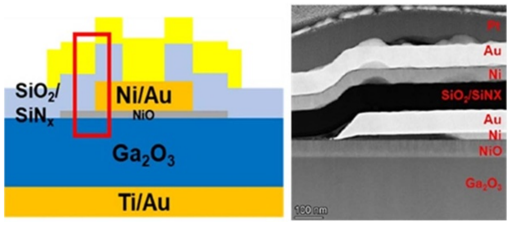

Figure 20. Cross-section image of heterojunction *p-n* Ga_2O_3 diode with BV of 13.5 kV. Reproduced from [7]. CC BY 4.0.

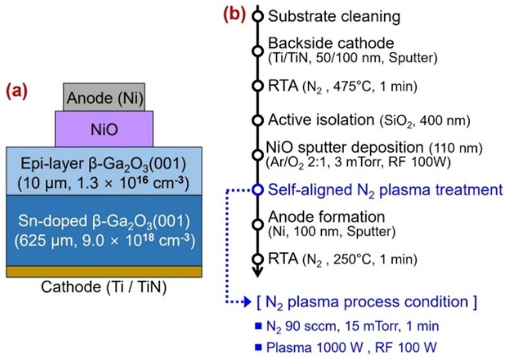

Figure 21. A self-aligned β-Ga_2O_3 HJDs with plasma treatment (a) Cross-sectional view and (b) process flow. Reprinted from [171], Copyright (2025), with permission from Elsevier.

Surface treatment proves effective in suppressing defects on the β-Ga_2O_3 surface. HJDs exhibit lower oxygen vacancies and higher BV of 1.54 kV by applying a surface preparation process involving a BCl_3/Cl_2-based ICP etch followed by a hot tetramethylammonium hydroxide (TMAH) treatment [200]. A controllable O_2 plasma interface treatment was developed to mitigate ion damage for high-performance p-NiO_x/β-Ga_2O_3 HJD [170]. A specific duration of O_2 plasma treatment enhances the density of strong interfacial NiOOH dipoles while tailoring the interfacial states of the Ni/NiO_x junction. These structural and electronic modifications lead to an increased surface hole concentration in NiO_x and a reduced ohmic contact resistance of 5.8×10^{-4} $\Omega\cdot cm^2$. Correspondingly, the treated devices achieve a BFOM of 0.675 GW cm^{-2}, representing a 209.63% improvement over untreated devices.

As illustrated in figure 21, a self-aligned nitrogen plasma treatment (SA-N_2) was employed for the fabrication of p-NiO/β-Ga_2O_3 HJD, enabling simultaneous concurrent nitrogen doping in both β-Ga_2O_3 and NiO [171]. The SA-N_2 plasma-treated HJD demonstrated improved BV from 1080 V to 1731 V, simultaneously maintaining a high on–off ratio exceeding 10^{11} and achieving a reduced $R_{on.sp}$. Moreover, SA-N_2 process holds the advantage of convenience and low cost, which can enhance the performance of β-Ga_2O_3 HJDs.

4.2. β-Ga_2O_3 HJDS with other metal oxide

In addition to p-type NiO, other p-type materials such as Cu_2O, SnO, Cr_2O_3, and $CuCrO_2$ are also suitable for gallium oxide heterojunction pn junction devices.

Cu_2O is also one of the earliest p-type oxide applied in β-Ga_2O_3 heterojunctions, with a bandgap of 2.1 eV and high hole mobility. Watahiki *et al* [178] first prepared the p-Cu_2O/β-Ga_2O_3 heterojunction diode in 2017. Results demonstrated a high breakdown voltage of 1.49 kV with a $R_{on.sp}$ of 8.2 m$\Omega\cdot cm^2$. The forward current density exceeded 100 A cm^{-2}, together with an ideality factor of 1.31, indicating the low conduction band offset at the interface between Cu_2O and Ga_2O_3 layers. Lately, p-Cu_2O/β-Ga_2O_3 HJDs with a double-layer design of Cu_2O were fabricated with a BV of 2430 V and a PFOM of 0.91 GW cm^{-2} by adjusting the hole concentration in Cu_2O layers [179]. However, Cu_2O is prone to degradation with high temperatures and specific atmospheres, necessitating in-depth discussion regarding the interface quality and long-term stability of the heterojunction.

SnO represents another promising p-type oxide for β-Ga_2O_3 heterojunctions. Despite its narrow bandgap ~0.7 eV, the BV of SnO/β-Ga_2O_3 heterojunction diode is not limited [182]. *p*-SnO/β-Ga_2O_3

heterojunction vertical diodes were fabricated with a p-type SnO grown by PAMBE on n-type (100) β-Ga_2O_3 [183]. The device exhibits stable switching properties with on/off ratios exceeding 10^6 and low $R_{on,sp}$ below 4 mΩ·cm^2 with a FOM of 0.37 GW cm^{-2}.

Other p-type materials, such as Cr_2O_3 and $CuCrO_2$, have also been investigated for β-Ga_2O_3 p–n HJD [187]. p-Cr_2O_3/β-Ga_2O_3 HJD were fabricated with the p-Cr_2O_3 film deposited via magnetron sputtering [185]. At room temperature, the device with a radius of 40 μm demonstrates a turn-on voltage of 1.7 V, a $R_{on,\,sp}$ of 4.6 mΩ·cm^2, and a BV of 1.96 kV, with an ideality factor as low as 1.07 achieved. The large-area p-Cr_2O_3/β-Ga_2O_3 heterojunction diode with optimized slanted-mesa edge termination technique exhibit a high BV of 1.78 kV, a forward current of 120 A and a PFOM of 0.511 GW cm^{-2} [186].

4.3. β-Ga_2O_3 heterojunctions with other p-type materials

Despite the high breakdown voltage and high on/off current ratios demonstrated by p-type metal oxides/β-Ga_2O_3 HJD, the amorphous nature of these p-type metal oxides may lead to trap states and dangling bonds, which limit the device performance [75]. Accordingly, alternative p-type materials have been explored for constructing high-performanceβ-Ga_2O_3 heterojunction devices.

To exploit the full potential of UWBG semiconductors in high-power applications, the use of p-type diamond and n-type Ga_2O_3 is considered for constructing the HJD by direct bonding [188], dry-transferred or heteroepitaxy growth [165]. Among all methods, heteroepitaxy enables the growth of thick films, leading to devices with the highest BV achievable [165]. An n-type β-Ga_2O_3/p-type (100) diamond heterojunction diode incorporating a lightly boron-doped p-diamond along with a high quality unintentionally doped Ga_2O_3 film was realized through ALD [165]. The differential resistance can achieve a low value of 34 mΩ cm^2 at 523 K. An avalanche BV of 186 V at 498 K indicates the diode's robust high-voltage endurance capability. p-diamond/β-Ga_2O_3 HJD fabricated by a direct-bonding technique at a low temperature exhibit a high rectifying ratio over 10^8 at $\pm$10 V and a leakage current lower than 10^{-12} A [188]. The ideality factor and barrier height of the p–n heterojunctions are derived to be appropriately 2.7 and 1.5 eV, respectively.

Additionally, investigations have also been conducted on p-hBN/β-Ga_2O_3 HJD [191]. The diodes exhibited rectification ratios of over 10^5 (300 K) and ~400 (475 K), the highest values reported for ultra-thin hBN-based p–n junctions. Moreover, the devices maintained stable and highly reproducible performance following multiple temperature cycles up to 475 K, indicating the reliable operation of the fabricated devices.

In addition to p-type ultra-wide bandgap semiconductors, a small number of studies have also explored heterojunction devices composed of other p-type materials and n-Ga_2O_3. The fabricated p-GaN/n-Ga_2O_3 diode by PAMBE obtains a low specific on-resistance of 2.4 mΩ·cm^2, a moderate on/off ratio of about 10^5, and stable high current densities of over 1 kA cm^{-2} [75]. The p-GaAs/β-Ga_2O_3 heterojunction diode via semiconductor grafting technique exhibits a high breakdown voltage of about 800 V and a PFOM of 126.5 MW cm^{-2} [195]. Using a semiconductor grafting approach, Gong *et al* successfully fabricated monocrystalline p-Si/β-Ga_2O_3 HJD with an ideality factor as low as 1.13 [197]. This outstanding performance was ascribed to surface oxygen enrichment on β-Ga_2O_3 surface, which passivates Si dangling bonds and suppresses interface defect density.

In summary, the advancement of heterojunction engineering has largely addressed the limitations of p-type β-Ga_2O_3. However, aside from NiO, the exploration and practical utilization of most other p-type semiconductor materials remain in the early stages of development.

4.4. Reliability of β-Ga_2O_3 HJDs

β-Ga_2O_3/p-type oxides HJDs have emerged as a practical solution to realize bipolar/vertical β-Ga_2O_3 power devices while avoiding the persistent challenge of reliable p-type doping in β-Ga_2O_3. However, the lattice mismatch can give rise to interfacial state, ionic/electronic reconstruction, and dangling bonds, raising serious reliability concern. The reliability of vertical β-Ga_2O_3 p–n junctions with p-type oxides remains a critical challenge due to their sensitivity to temperature, electrical stress, and radiation-induced defect dynamics.

4.4.1. Thermal and electrical effect

For β-Ga_2O_3 HJD, thermal and forward stress induces complex dynamic degradation [202]. Injected minority holes can occupy trap states, triggering trap-filled limit and SCLC behavior, which temporarily lowers $R_{on,sp}$ [203]. There have been some investigations on the majority carrier (electron) traps [204] and minority carrier traps in the β-Ga_2O_3 p–n heterojunction, yet quantitative assessment of reliability of bipolar diodes and trapping effect is needed.

High-temperature induced degradation is closely associated with deep-level defects in β-Ga_2O_3 bulk materials and at oxide/semiconductor interfaces. For NiO/β-Ga_2O_3, the noise spectral density exhibits the $1/f$-type curves near room temperature (RT) which evolved to show signatures of Lorentzian components at elevated temperatures and at higher current levels, characterized by LFN spectroscopy [205]. Results of thermal cycling between RT and 550 °C show an initial leakage current increase which stabilizes after sustained thermal load, due to the formation of the spinel $NiGa_2O_4$ layer between NiO and β-Ga_2O_3 [166]. Notably, the introduction of a $NiGa_2O_4$ p-type interfacial layer enhances the electrical stability of NiO/β-Ga_2O_3 HJD, achieving an increased BV of 1.2 kV. For p-$CuGaO_2$/β-Ga_2O_3 heterojunction, the surface roughness of the p-$CuGaO_2$ layer may increase at higher temperatures, potentially impacting the heterojunction interface. Three deep traps were extracted by DLTS from 100–700 K. The higher density and larger capture cross-section suggest that it could play a major role in degrading the performance at elevated temperatures, by increasing leakage currents and reducing carrier lifetimes [206].

The thermal effects occurring during electrical breakdown will induce thermo-mechanical failure in Ga_2O_3 devices. In literature, fin diodes fabricated on (001) β-Ga_2O_3 substrates exhibited cracking along the [010] direction after destructive breakdown [120, 139]. This cracking was suggested to be due to thermo-mechanical failure of the (100) cleavage planes due to heat generation during breakdown.

At the device-level, forward-bias stress induced a negative turn-on voltage shift in HJDs, with the shift magnitude scaling with stress current density; reverse-bias stress produced the opposite trend. Such V_{on} shift was attributed to an electron trap at EC–0.46 eV, likely originating from native point defects in β-Ga_2O_3 near the heterointerface.

The small V_{on} shift below 0.1 V was comparable to that reported in SiC and GaN p–n junction diodes [199]. Moreover, at the circuit-level switching reliability, after 10^7 switching cycles, the HJD exhibited a V_{on} reduction of up to 0.25 V and a differential on-resistance drop of 36% [204]. Such shifts were fully recoverable and governed by deep-level trapping/de-trapping with a time constant of 4.2 ks.

4.4.2. Radiation effect

β-Ga_2O_3 p–n heterojunction rectifiers provide superior BV performance relative to Schottky rectifiers, while the presence of p-type materials does affect some aspects of the response to radiation, such as neutron, proton and ion irradiation.

Neutron [207] and proton irradiation [175, 208] introduce deep levels (E_C-0.75 eV) in bulk or degradation at heterojunction interface, reducing carrier concentration and increasing trap density both in the β-Ga_2O_3 drift layer and near the hetero-interface. After 1 MeV neutron irradiation with a fluence of 1×10^{14} n cm^{-2}, the forward current density of β-Ga_2O_3 HJD decreased by 23%, due to carrier removal effect [207]. The synergistic impact of reverse bias stress and 3 MeV proton irradiation on the β-Ga_2O_3 p–n diode indicates that the increase in acceptor-like traps (E_C-0.75 eV) within drift layer results in the carrier concentration reduction, which in turn leads to a decrease in forward current [208].

Moreover, the irradiation fluence dominates the degradation severity for HJDs, as shown in figure 22. With 15 MeV proton irradiation, vertical NiO/β-Ga_2O_3 rectifiers showed a BV drop from 4.3 kV to3.7 kV for a fluence of 10^{13} cm^{-2}, and to 1.93 kV at 10^{14} cm^{-2} [209]. For high fluence samples, annealing up to 400 °C further increased reverse leakage due to deterioration of the contacts, whereas low-fluence devices largely recovered their initial carrier density. The carrier removal rate in β-Ga_2O_3 was extracted to be 190–1200 cm^{-1} within this fluence range, similar to that of SBD without a p-type NiO layer.

β-Ga_2O_3 HJDs exhibit superior SEB performance than SBDs, because the introduction of a p-type layer enables the heterojunction to alleviate electric field crowding and facilitate hole extraction. For high energy ion-irradiation, the thicker p-type region in HJDs could further alleviate the electric field crowding effect exacerbated by the heavy-ion strike because of the extension of charge distribution in the p-type region [210]. The SEB threshold was raised to 250 V by thickening the NiO layer to 300 nm. By performing bias voltage-dependent experiments with 1.35 GeV high-energy Ta ion irradiation, the catastrophic burnout in irradiated HJD is identified in two distinct regions [211]. Region I (p-NiO/n^--Ga_2O_3) is characterized by trap-assisted electric field breakdown, whereas Region II (n^--Ga_2O_3/n^+-Ga_2O_3) is characterized by thermally driven damage arising from charge accumulation. Therefore, improving thermal management and suppressing the corresponding traps is essential for β-Ga_2O_3 HJDs.

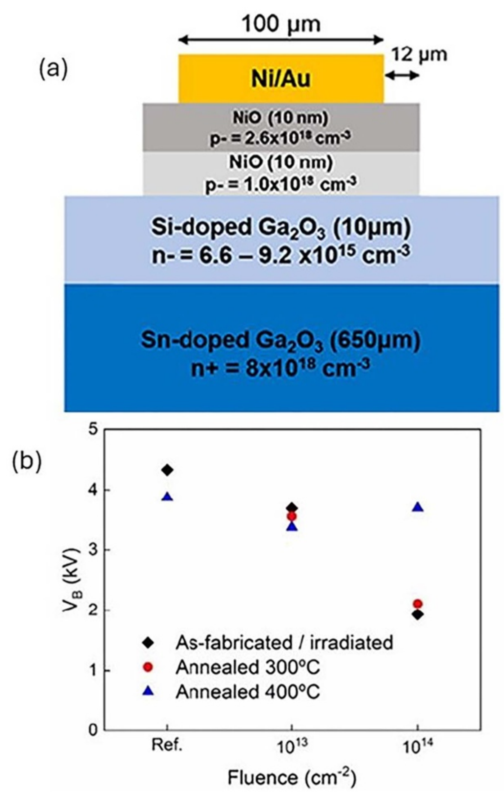

Figure 22. Radiation hardness of NiO/Ga_2O_3 rectifier: (a) Device structure and (b) change in reverse BV with proton dose and the subsequent anneal temperature. Reproduced from [209]. CC BY 4.0.

5. Vertical β-Ga_2O_3 power transistors

Extensive research efforts have been devoted to unipolar n-channel device architectures that eliminate the requirement for p-type layers. Among these configurations, two major categories have garnered considerable attention: vertical fin field-effect transistors (FinFETs), which employ fin-shaped channels to improve gate electrostatic control, and CBL-based devices, including current aperture vertical electron transistors (CAVETs), vertical diffused barrier FETs (VDBFETs), and U-shaped trench-gate MOSFETs (UMOSFETs).

5.1. FinFET structure

Vertical FinFETs transfer the fin-channel concept from lateral to vertical stack, enabling stronger gate control and promising high BV due to the thick β-Ga_2O_3 drift layers. A typical vertical FinFET structure consists of an n^+ source region connected to a fin-shaped channel, a lightly doped n^- drift layer, and an n^+ substrate for current spreading [6]. The typical fabrication process of vertical FinFETs initials with the growth of a β-Ga_2O_3 epitaxial stack with an n^- drift layer on an n^+ substrate. Fin channels are then defined by anisotropic ICP etching with optimized sidewall morphology and metal (Cr and Ni) or dielectric as hard mask. High-k dielectrics such as Al_2O_3 or HfO_2 are deposited by ALD, followed by the gate metal formation. A spacer layer of SiO_2 was deposited by PECVD serving as the isolation between the gate and source pads.

Vertical FinFETs are crucial to achieve enhancement-mode operation in the absence of the effective p-type doping. Normally-off operation was successfully demonstrated by reducing a fin width (W_{fin}) of FinFETs. The gate dielectric and electrode wrap around the fin sidewalls to enhance electrostatic control, and the drain contact is located at the backside of the substrate. Compared to lateral FETs, the vertical topology inherently contributes to higher area efficiency and more uniform electric field distribution. The characteristics of devices such as on-resistance, drain current, and short-channel effects induced drain-induced barrier lowering (DIBL), which degrades breakdown characteristics and threshold stability, were significantly influenced by the key geometric factors such as channel length and width [212, 213]. In figure 23, process variations by factors such as fin height, oxide thickness, gate height, and doping concentration can introduce fluctuations, causing dispersion in leakage current.

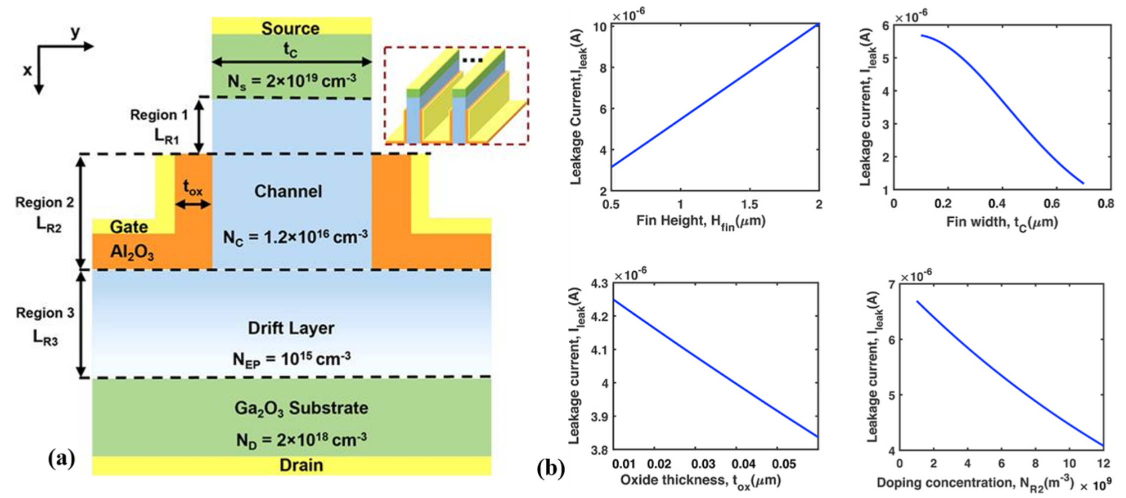

Figure 23. (a) Device structure of vertical FinFETs. (b) Influence of fin height, fin width, oxide thickness, and doping concentration on leakage current. Reproduced from [213].

Table 7. Summary of key parameters of vertical Ga_2O_3 power transistors.

Devices	Subs. orientation	Epi. (μm)	BV (kV)	$R_{on,sp}$ (mΩ cm^{-2})	$I_{DS,max}$ (A cm^{-2})	V_{th} (V)	FOM (MW cm^{-2})	References
FinFET	(011)	85	>10	289	15.1	0.65	350	[6]
FinFET	(100)	1.5	0.26	NA	0.2	4.2	NA	[222]
FinFET	(001)	10	1.605	5.5	0.6	4	470	[223]
FinFET	(001)	10	2.655	25.2	0.1	1.8	280	[224]
CAVET	(001)	10	<0.03	31.5	0.42	−54	0.03	[217]
CAVET	(001)	10	0.263	135	0.026	4	0.52	[219]
VDBFET	(001)	10	0.072	NA	0.15	7	NA	[225]
UMOSFET	(010)	0.6	0.101	5	1560	5	2	[226]
UMOSFET	(001)	10	0.985	24.37	>1	>4	40	[227]
UMOSFET	(001)	10	1.028	87.6	>200	14.4	12.06	[228]
UMOSFET	(001)	10	0.455	10.4	0.702	4.2	19.91	[221]

As shown in table 7, β-Ga_2O_3 FinFETs demonstrate superior breakdown voltage (over 10 kV) compared to other architectures. To date, nearly all reported β-Ga_2O_3 FinFETs have been fabricated on commercially available (001) Ga_2O_3 substrate. However, the on-axis (100) plane, characterized by the lowest dangling bond density among primitive index planes, cannot be employed as fin sidewalls, primarily due to the ∼104° angle between the (100) and (001) planes, becoming a key limitation of Ga_2O_3 (001) substrates [214].

Vertical FinFET with high breakdown and low conduction loss requires precise control on doping concentration and compensation levels in the drift layer with a thickness of tens of micrometers. Wakimoto *et al* reported a normally-OFF multi-fin vertical transistors in which an *in-situ* N-doped well was incorporated during HVPE growth. The devices yielded high electron mobility (∼100 cm^2 (V^{-1} s^{-1})) and stable enhancement-mode behavior [215]. Recently, a breakdown voltage exceeding 10 kV has been demonstrated in multi-fin vertical FETs, which were fabricated on a thick (∼85 μm) epitaxial layer with low-donor-concentration (1.8 × 10^{15} cm^{-3}) grown by HVPE on a (011)-oriented β-Ga_2O_3 substrate [6].

5.2. CAVET structure

Vertical Ga_2O_3 CAVETs draw inspiration from commercially SiC double-implanted MOSFETs and GaN CAVETs [216]. As shown in figure 24, CBL structure typically formed through ion implantation (e.g., Mg or N), creates a high-resistance region that restricts current flow to an aperture with gate modulation. The difference between gate length and aperture length (L_{go}) determines the extent of the controllable channel and thereby influencing threshold voltage of device [217, 218].

The fabrication process of device began with a Sn-doped β-Ga_2O_3 (001) substrate and a lightly Si-doped layer grown by HVPE. Mg (or N) and Si were implanted to establish the CBL and the channel, respectively. Source probing pads were used for minimizing pad leakage current.

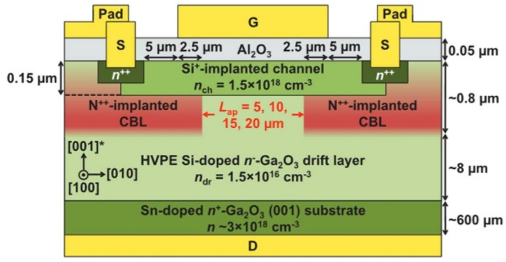

Figure 24. Cross-sectional schematics of a vertical Ga_2O_3 CAVET with nitrogen-implanted CBLs. Reprinted from [218], with the permission of AIP Publishing.

CAVETs feature an unetched gating surface and offer relatively straightforward integration. Their operation mode (enhancement- or depletion-mode) can be tuned by adjusting the channel doping concentration [219]. For instance, depletion-mode CAVETs were fabricated with a channel concentration of 1.5×10^{18} cm^{-3} on a β-Ga_2O_3 (001) substrate, exhibiting a drain current density of 0.42 kA cm^{-2}, a specific on-resistance of 31.5 mΩ·cm^2, and an output current on/off ratio of over 10^8 [217], in table 7. To achieve enhancement-mode operation, the doping concentration of the channel was reduced to 5×10^{17} cm^{-3}. *E*-mode CAVETs were developed on a single-crystal β-Ga_2O_3 (001) substrate [219]. The devices delivered a high output current on/off ratio of 2×10^7 despite a nonideal MOS interface that limited the maximum drain current density to $<$0.1 kA cm^{-2}.

5.3. VDBFET and UMOSFET structure

In addition to CAVETs, VDBFETs and UMOSFETs constitute the second major family of CBL-based vertical transistors [220]. Both architectures contain a compensated region to block current in the off-state and form a conduction channel with appropriate gate bias. In both architectures, acceptor doping by Mg or N implantation introduces deep-level compensating centers that counterbalance n-type carriers, resulting in the establishment of a high-resistivity layer without true p-type conductivity—commonly characterized as quasi-p-type behaviors. This mechanism not only emulates the blocking functionality of a p–n junction but also remains compatible with the unipolar nature of β-Ga_2O_3. The main difference between these two structures is that the UMOSFET features a U-shaped gate trench structure.

For VDBFET fabrication, Zeng *et al* pioneered the development of a VDBFET using Mg doping spin-on-glass as a dopant source and thermal diffusion to form the CBL, achieving an ON/OFF ratio of 10^9 with BV of 72 V [225]. This innovative approach effectively overcame the challenges of Mg implantation and high-temperature annealing. However, unintentional incorporation of residual Cl and N impurities introduced during HVPE growth degraded the off-state leakage current, illustrating the delicate balance between epitaxial doping control and electrical isolation. The results highlight that precise management of background doping and impurity gettering during growth becomes indispensable for reproducible CBL characteristics.

In figure 25, the CBL of UMOSFETs can be realized by high temperature oxygen annealing [220]. The fabricated UMOSFET showed normally off with a V_{th} of 11.5 V and $I_{on/off}$ ratio of 6×10^4. However, the relatively shallow depletion layer constrained the BV to less than 200 V. Via modulation of the implanted nitrogen ion concentration, a UMOSFET with a practical V_{th} of 4.2 V was attained, accompanied by an enhanced BV of 455 V [221]. Recently, by optimizing the N-ion implantation concentration and activation annealing temperature, the fabricated device achieved the BV over 985 V with 1100 °C and 1.3 kV with 1200 °C, respectively [227].

In summary, FinFETs offer the greatest dimensional scaling potential, with BV exceeding 10 kV already demonstrated. However, the fabrication process demands the highest lithographic precision. CAVETs and VDBFETs strike a balance between process complexity and cost, with scalability governed by doping control accuracy. UMOSFETs require breakthroughs in trench etching technology to extend scalability toward higher voltages.

5.4. Reliability of vertical transistor

Compared with vertical SBDs and pn HJDs, reliability research on vertical β-Ga_2O_3 transistors is relatively in its early stages. The quality of gate stack, thermal-induced effect, and ion-induced effect are crucial for the stability of vertical β-Ga_2O_3 transistors.

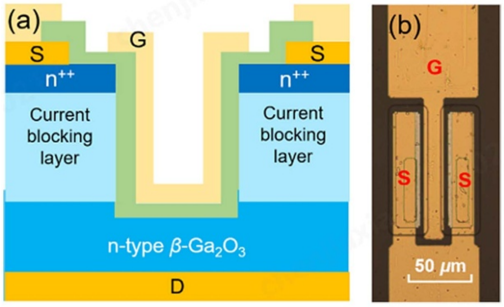

Figure 25. (a) Schematic cross sections and (b) Optical micrograph of a β-Ga_2O_3 UMOSFET with CBL realized by oxygen annealing. Reprinted from [220], with the permission of AIP Publishing.

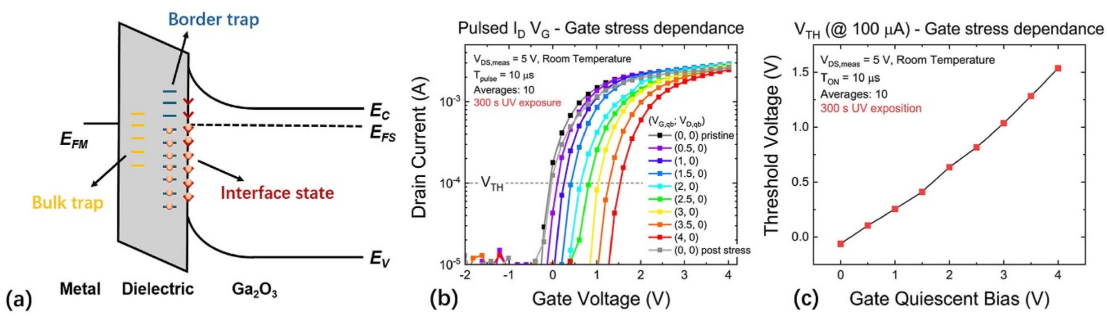

Figure 26. (a) Schematic band diagram and traps with different location of gate dielectric/β-Ga_2O_3 MOS structure. (b) Pulsed I_D–V_G experiment as a function of a different quiescent bias at RT (25 °C). (c) Extracted V_{TH} at a current level of 10^{-4} A. Reproduced from [233].

5.4.1. Gate stability

The gate stacks of various vertical β-Ga_2O_3 devices adopt the MOS structure, and the quality of the gate dielectric and its interface directly determines the device gate stability, such as V_{th} instability and high gate leakage.

Although the BV and $R_{on,sp}$ of β-Ga_2O_3 FETs have been effectively optimized, they remain susceptible to gate dielectric instability [229, 230]. Interface state, oxide trap, and border traps play key roles in determining the magnitude and time dependence of bias-temperature instabilities in MOS gate stack, as shown in figure 26(a). Typically, β-Ga_2O_3 is grown in a dedicated reactor and then transferred to a separate system for dielectric deposition [231]. However, ambient contaminants introduced during the transfer accumulate on the surface, requiring extensive chemical pre-treatments. This not only prolongs the processing time but also introduces adverse side effects that degrade the interface quality and may cause process incompatibility.

Such issues can be effectively addressed by an *in-situ* growth approach, where the dielectric is deposited in the same chamber as the β-Ga_2O_3 epilayer. Time dependent dielectric breakdown characterization shows that the *in situ* Al_2O_3 deliver a 10 year lifetime at a stress field of 3.5 MV cm^{-1}, with a catastrophic breakdown field of 7.8 MV cm $^{-1}$ [232].

Interface quality between the gate dielectric and the vertical channel also plays a crucial role in device performance and V_{th} reliability [213, 230]. Moreover, defects induced by dry etching on sidewall surfaces of vertical Ga_2O_3 fin channel and horizontal surface lead to device instability such as threshold voltage instability and dynamic switching behaviors. Trapping and de-trapping mechanisms at the interface between the gate dielectric and the vertical fin channel are proved to cause an irreversible positive V_{th} shift with gate bias stress, which has critical implications for device reliability [229, 230]. In figures 26(b)–(c), positive quiescent bias results in a rightward shift of the transfer curve, indicating electron trapping at oxide or interface traps. Based on electro-optical model, the thermally activated trapping process of vertical FinFET was demonstrated, with thermionic barrier energy equal to 0.44 ± 0.08 eV, due to the injection of the electrons in oxide captured by border traps [233].

To obtain the high-quality interface, wet-etching process and nitrogen radical irradiation were employed to recover damage on Ga_2O_3 surfaces and improve the device performance [214]. The ion damage and sidewall roughness are demonstrated to be supressed by H_3PO_4 or HF, leading to negligible hysteresis [234]. Moreover, as an alternative to HVPE, MOCVD can be grown with sub-nanometer surface roughness and hence avoid postgrowth CMP.

Meanwhile, significant V_{th} shifts were revealed by dynamic characterization with pulsed operation, indicating persistent interface charge trapping [217]. The results emphasized that robustness of dielectric and interface engineering were the decisive bottlenecks for CAVET scalability. Optimized implantation recipe and annealing schedules are unavoidably to achieve abrupt, stable CBL profiles while suppressing diffusion tails that undermine off-state blocking. On the gate side, high-k dielectrics with greater breakdown strength (e.g., HfO_2, AlN or multilayer stacks) and pre-ALD surface treatments can effectively reduce trap state density and alleviate dynamic instability. During deposition of gate dielectric using ALD, the thick crystalline Al_2O_3 interlayer on β-Ga_2O_3 can effectively decreased interface state [231].

5.4.2. Thermal reliability

Since the low thermal conductivity of β-Ga_2O_3 results in high thermal resistance, thermal management is critical to the reliability of vertical FETs.

Due to the anisotropy of the Ga_2O_3 thermal conductivity, electro-thermal modeling for vertical FinFET shows that a 20% reduction with the temperature rise is possible by devices on a (010)-oriented substrate as compared to the tested devices built on a (001) substrate [235]. The Ga_2O_3 FinFET with diamond-gate (DG-FinFET) enhance heat dissipation due to the high thermal conductivity of the diamond material [236]. In package level, top- and double-side cooling of vertical FinFETs are considered as effective strategies for maintaining junction temperatures below 200 °C [237]. A fin spacing greater than 8 μm are recommended to mitigate thermal crosstalk due to the employment of SiO_2 as a dielectric spacer which has a poor thermal conductivity.

Thermal management strategies at the device level are required in order to achieve high power operation. Double-side cooling in combination with a heat spreader can suppress the device's thermal resistance from 24.5 to 4.86 mm ∘C/W, allowing for a high-power-density CAVET device [216]. However, double-sided cooling is far more difficult to implement from an engineering perspective. For this reason, thermally conductive dielectric such as AlN for vertical trench-fin MOSFETs, is an effective method for aiding thermal spreading. In addition, bonding thermal spreaders to its upper surface can lead to substantial enhancements in thermal performance [237].

5.4.3. Ion-implantation induced effect

Vertical β-Ga_2O_3 transistors remain at an early developmental stage. In contrast to vertical diodes, research on irradiation-induced ion damage is scarce. Additionally, ion implantation damage introduced during processing is another key factor impacting device reliability.

High-energy ion implantation induces lattice displacement damage, as well as the thermal diffusion of dopants and point defects. Even in the low-dose ion implantation regime—where phase transformations are not anticipated—the accumulation of lattice disorder and its thermal evolution in β-Ga_2O_3 remain critical to device performance [238]. The *in situ* dynamic annealing effect of high temperature implantation effectively reduces implantation-induced damage, and enhances impurity activation, improving the overall performance of the N-implanted CBLs in β-Ga_2O_3, with elevated BV and stable leakage current [239].

There are also many ion-implantation induced issues remaining to be solved for β-Ga_2O_3 CAVETs, such as low BV, small gate voltage swing, high reverse leakage, and high R_{on} device due to the lack of suitable p-type doping [218]. Early studies by Wong *et al* demonstrated the realization of CBL by Mg-ion implantation, achieving isolation between the source and drain. However, the unoptimized Mg profile caused redistribution during post-annealing, leading to high off-state leakage [240]. Subsequent efforts utilizing N implantation achieved tighter confinement and improved on/off ratios while avoiding Mg-related diffusion issues [219].

For UMOSFET, in addition to extrinsic dopants, defect-driven CBL formation has emerged as a promising route. Zhou *et al* proposed a high-temperature oxygen annealing process ($\sim$ 1200 °C) to generate Ga vacancies that acted as compensating centers, thereby forming high-resistivity regions suitable for current blocking [220]. The purely thermal method eliminates implantation-related damage and simplifies process integration, offering a potential low-cost path for CBL fabrication. Nevertheless, the reproducibility and scalability of epitaxial layers remain to be validated. The performance of these CBL-based UMOSFET architectures ultimately depends on the uniformity, stability, and depth control of the compensated region [227].

In contrast, an *in situ* epitaxially grown insulating layer can be flexibly fabricated, which circumvents the inherent conflict between the high diffusivity of acceptors in β-Ga_2O_3 at elevated temperatures and the high-temperature requirements for crystal recovery and dopant activation following ex situ ion implantation. Thus, *in situ* acceptor doping methods (e.g., N or Mg doping) for CBL fabrication represent a promising pathway toward high-performance vertical β-Ga_2O_3 devices [241]. In brief summary, for reliability improvement, vertical β-Ga_2O_3 transistor progress is paced by three coupled levers: drift-layer quality together with its charge control, gate-stack/interface engineering to suppress trapping and DIBL, and thermal path design spanning device and package [216, 242]. Co-optimization across these levers has already moved the architecture from feasibility to kilovolt-class *E*-mode operation, with reliability and thermal robustness now becoming the primary gates to application-level deployment.

6. Future outlooks

6.1. P-type conduction issues in β-Ga_2O_3

The absence of viable p-type conductivity in β-Ga_2O_3 is regarded as the critical challenge that prevents the realization of conventional p–n junction-based devices such as IGBTs [243]. Unlike *n*-type doping, achieving stable p-type conductivity in β-Ga_2O_3 has proven extremely challenging. The difficulty arises from a low energy level of valence-band maximum (VBM) and flat band dispersion at VBM in β-Ga_2O_3 [244–246]. Consequently, β-Ga_2O_3 shows a low hole mobility (theoretically room-temperature value approximately 1–2 $cm^2V^{-1}\,s^{-1}$) [246, 247], and common dopants in β-Ga_2O_3 exhibit deep acceptor levels (larger than 1 eV) [248, 249]. These inherent limitations make conventional substitutional doping strategies ineffective for achieving reliable p-type conduction.

6.1.1. Short-term p-type: heterojunction

Regarding the p-type doping bottleneck, forming heterojunctions with alternative p-type oxides has emerged as the short-term solution. This approach leverages mature p-type wide-bandgap materials such as NiO and Cu_2O, to construct p–n heterojunctions with n-type Ga_2O_3 [7]. High-performance rectifiers and field-effect transistors with BV exceeding 10 kV have been realized based on NiO/β-Ga_2O_3 heterostructures. However, lattice and thermal expansion mismatches between dissimilar materials introduce high-density interface states, which causes carrier trapping, Fermi-level pinning, and device failure with high-field operation. Further optimizations are required to reduce the interface states for these p–n heterojunctions.

6.1.2. Medium-term: alloying strategy and defect engineering

Given the low energy level of VBM in β-Ga_2O_3, an alternative medium-term strategy for p-type conduction is to elevate the VBM energy of β-Ga_2O_3 by alloying other elements. For example, the VBM energy levels of β-Ga_2O_3 are significantly evaluated by alloying Bi_2O_3 [250] and NiO [251]. The band dispersion at the VBMs becomes steeper, and the hole effective mass reduces in β-$(Bi_xGa_{1-x})_2O_3$ [250]. Zha *et al* conducted a detailed first-principles study of the band structure and carrier- transport properties of alloys composed of various metal elements and β-Ga_2O_3, identifying the β-$(Rh_xGa_{1-x})_2O_3$ alloy may exhibit p-type conductivity [246, 252], as illustrated in figure 27. Moreover, N-doped β-Ga_2O_3 achieved by a phase transition from GaN to β-Ga_2O_3 possesses low formation energy, thereby with good N dopant solubility and low activation energy of N acceptors (0.355 eV) [253].

In addition to alloying strategies, defect engineering is also found to be an effective route for achieving p-type conduction in β-Ga_2O_3. Chikoidze *et al* observed enhanced p-type conduction in the MOCVD-grown β-Ga_2O_3 films after annealing in the oxygen atmosphere, with hole concentrations up to 10^{17} cm^{-3} and mobilities larger than 10 cm^2 $(V{\cdot}s)^{-1}$. The behavior is attributed to the complex defect consisting of Ga vacancies ($V_{Ga}{}^{-}$) and O vacancies (Vo^{++}), and the Coulomb interaction between defects lowers the acceptor level [254].

Ion implantation offers another method to introduce acceptor elements (such as P, Ni, N) locally during device fabrication, followed by annealing to repair damage and activate the dopants. Implantation can create non-equilibrium chemical states, which cannot be accessible via equilibrium growth, enabling transient or localized p-type behavior. Horng *et al* have demonstrated p-type layers using different doses phosphorus-ion implantation combined with optimized annealing, achieving a p-type layer on a sapphire substrate with hole concentrations around 1×10^{17} cm^{-3} and mobilities of $\sim$0.2 cm^2 $(V{\cdot}s)^{-1}$ [255]. Shimizu *et al* obtained p-type conductivity by Ni implantation combined with a two-step O_2 plasma plus thermal annealing process, and further demonstrated p–n diodes with Ni-doped Ga_2O_3/n-type Ga_2O_3 [256]. The above p-type doping achieved by ion implantation might also be regarded as a kind of defect engineering. The non-equilibrium process is utilized to generate various defects, and the interactions between these defects reduce the acceptor level.

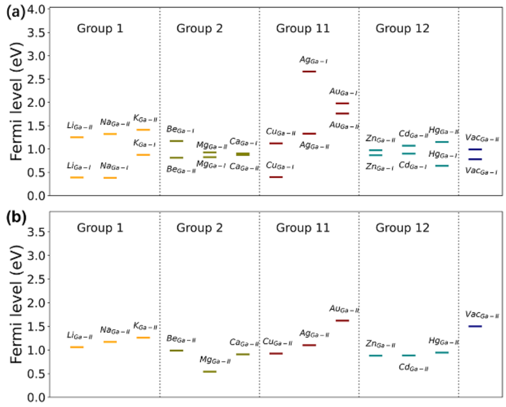

Figure 27. The acceptor levels for possible dopants in (a) β-($Rh_{0.25}Ga_{0.75})_2O_3$; (b) β-($Rh_{0.5}Ga_{0.5})_2O_3$ configurations. Reproduced from [246].

Although p-type conductivity in β-Ga_2O_3 has been reported via elemental alloying and defect engineering, further experimental verifications are still required, especially regarding the long-term stability of its p-type conduction.

6.1.3. Long-term: in-situ p-type doping

In-situ acceptor doping during film growth is conceptually attractive because it enables uniform substitutional incorporation of acceptors without causing lattice damage. Both first-principles calculations and experimental reviews emphasize that although *in-situ* methods can generate acceptor-like states or compensate unintentional donors, the ionization energies of acceptors in β-Ga_2O_3 are typically very deep, resulting in extremely low thermally activated hole concentrations at room temperature. Candidate acceptors in the previous investigation include Zn, Mg, N, and other theoretically predicted dopants [257]. Jesenovec *et al* grew Zn-doped β-Ga_2O_3 single crystals and found that Zn-doped β-Ga_2O_3 exhibits extremely high resistivity (10^{11}–10^{14} $\Omega\cdot$cm), indicating a highly insulating state rather than p-type conduction [258]. Similarly, Feng *et al* investigated Mg *in-situ* doping in MOCVD-grown β-Ga_2O_3 thin films and also reported that the films remained highly resistive rather than p-type [259]. Ghadi *et al* precisely determined the acceptor level of N by DLOS, which proved that the N acceptor lay 1.9 eV above the VBM, indicating that N was a very deep acceptor and cannot support p-type conduction [260].

Recent work has demonstrated p-type conductivity in N-doped β-Ga_2O_3, achieving a high hole concentrations (>1 × 10^{18} cm^{-3}) and a mobility of 0.47 cm^2 $(V\cdot s)^{-1}$. The study suggests that N substituting O (N_O) can create a relatively shallow acceptor level. This work also demonstrates that it is significant for p-type conduction to eliminate other compensating defects in the film [261]. Nevertheless, reproducible high-mobility hole transport remains rare and typically exists only at the edge of detectability, with very low concentrations and limited thermal stability. Achieving p-type conductivity in β-Ga_2O_3 through *in-situ* p-type doping still requires more attempts and the exploration of novel mechanisms.

6.2. Thermal management

The inherent low thermal conductivity of β-Ga_2O_3 (10–30 W $m^{-1}\cdot$K) poses a critical challenge for high-power device thermal management. This intrinsic limitation demands a co-design approach that combines device-level innovations like substrate thinning and heterogeneous integration [262] with packaging-level methods, such as double-sided cooling and flip-chip [263].

6.2.1. Device-level thermal management

Reducing the thickness of the native β-Ga_2O_3 substrate shortens the heat-spreading path and lowers the thermal resistance. Substrate thinning from 500 to 85 μm via grinding/polishing reduces the R_{on} from 174 to 112 mΩ, boosting forward and surge current from 20 to 29 A, and the thermal resistance of packaged device's thermal resistance drops significantly to 2.21 K W^{-1}, comparable to commercial SiC SBDs [264]. However, precisely control the mechanical thinning of β-Ga_2O_3 remains a challenge for large-scale manufacturing. Specifically, excessively thinned substrates compromise the mechanical stability of semiconductors, rendering the fragile wafer and thereby adversely affecting subsequent device fabrication processes.

Another method involves integrating a high-conductivity substrate (like SiC, diamond or AlN) to act as a heat sink, rapidly removing heat from the active region, including during heteroepitaxial growth and heterogeneous integration [10, 265]. The primary challenge in heteroepitaxy is the significant mismatch in lattice and thermal expansion coefficients between β-Ga_2O_3 and substrates, which results in high defect densities, poor crystal quality, and problematic interfacial thermal resistance (TBR) [266]. For instance, an AlN interlayer significantly enhances interfacial bonding and thermodynamic stability between β-Ga_2O_3 and diamond, with thermal conductivity increasing from 5.5 to 6.0 W m^{-1} K [267]. Moreover, combination of diamond substrate and the AlN interlayer can mitigate the self-heating effect. Thus, heterogeneous integration involves physically transferring a prefabricated, thin β-Ga_2O_3 layer onto a high-thermal-conductivity carrier substrate, which often involves sophisticated techniques such as ion cutting, wafer bonding and the implement of van der Waals interfaces [268].

6.2.2. Package-level thermal management

Advanced packaging techniques are critical for efficiently extracting heat from the device to the system level. Recent works focus on double-sided cooling, flip-chip architectures, and thermally enhanced packaging structures. Wang *et al* demonstrate vertical β-Ga_2O_3 SBDs with over a 15 A current and BV of 600 V using double-side-packaging [269]. Guan *et al* proposed an advanced double-sided cooling flip-chip structure that adds a diamond layer on top of the device [270]. When integrated with a water-cooling equipment package, the maximum device temperature dropped to 186 °C at a power density of 6.8 W mm^{-1}. Liu *et al* compared various thermal-management schemes and concluded that flip-chip packaging is the most effective strategy for β-Ga_2O_3 FETs [271]. By using an appropriate carrier in the flip-chip package, the temperature rise at 2 W mm^{-1} power density can be reduced by ∼91% compared with the baseline device. The study also noted that flip-chip heterogeneous integration enhanced heat dissipation without compromising the native β-Ga_2O_3 substrate.

7. Summary

This review has discussed critical aspects of β-Ga_2O_3 technology for power electronics, encompassing epitaxial growth, vertical device architectures, and potential optimization strategies for p-type doping and thermal management. β-Ga_2O_3 devices are positioned to play a significant role in next-generation power converters. Prior to its large-scale commercialization, the following critical challenges must be addressed.

Epitaxial growth techniques like HVPE, MOCVD, and MBE have advanced vertical device architectures, laying the groundwork for high-performance β-Ga_2O_3 power electronics. Among them, HVPE excels in mass production with low cost, MOCVD enables precise control with favorable growth rate, and MBE facilitates high-quality film fabrication. To promote their practical applications, β-Ga_2O_3 epitaxy still needs to continuously reduce defect density and ensure uniformity, especially on large-size substrates.

Vertical devices have shown rapid performance advances, with BV over 10 kV demonstrated. However, their performance remains far below the intrinsic material limits, mainly due to the material defects, immature processes and unclear reliability mechanisms. One of key priorities is identifying and suppressing killer defects that degrade breakdown characteristics. Meanwhile, improving interface quality and relieving electric field crowding via efficient edge terminations are also critical to boost blocking voltages. Additionally, a low-resistance Au-free ohmic contacts is essential to reduce $R_{on,sp}$ and conduction losses.

Alongside advancements in β-Ga_2O_3 material and device technology, addressing p-type doping and thermal management remains a pivotal challenge. Unreliable p-type doping restricts cmOS compatibility, and causes device reliability issues. Device and package-level thermal management will be essential for the suppression of self-heating. Developing integrated structures and exploring heterostructures can further boost device performance.

Through interdisciplinary collaboration, β-Ga_2O_3 vertical devices could transform power electronics and meet global energy demands. As their performance matures, they are expected to engage in increasingly robust competition with established Si and SiC technologies in the coming years.

Acknowledgment

This work was supported by National Natural Science Foundation of China (Grant No. 52131303), Guangdong Basic and Applied Basic Research Foundation (2026A1515010747), Shenzhen Science and Technology Program (Grant No. QNXMC20250701100535022) and the Shenzhen Pinghu Laboratory Project (Grant No. 925050).

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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